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SEPTEMBER 2016

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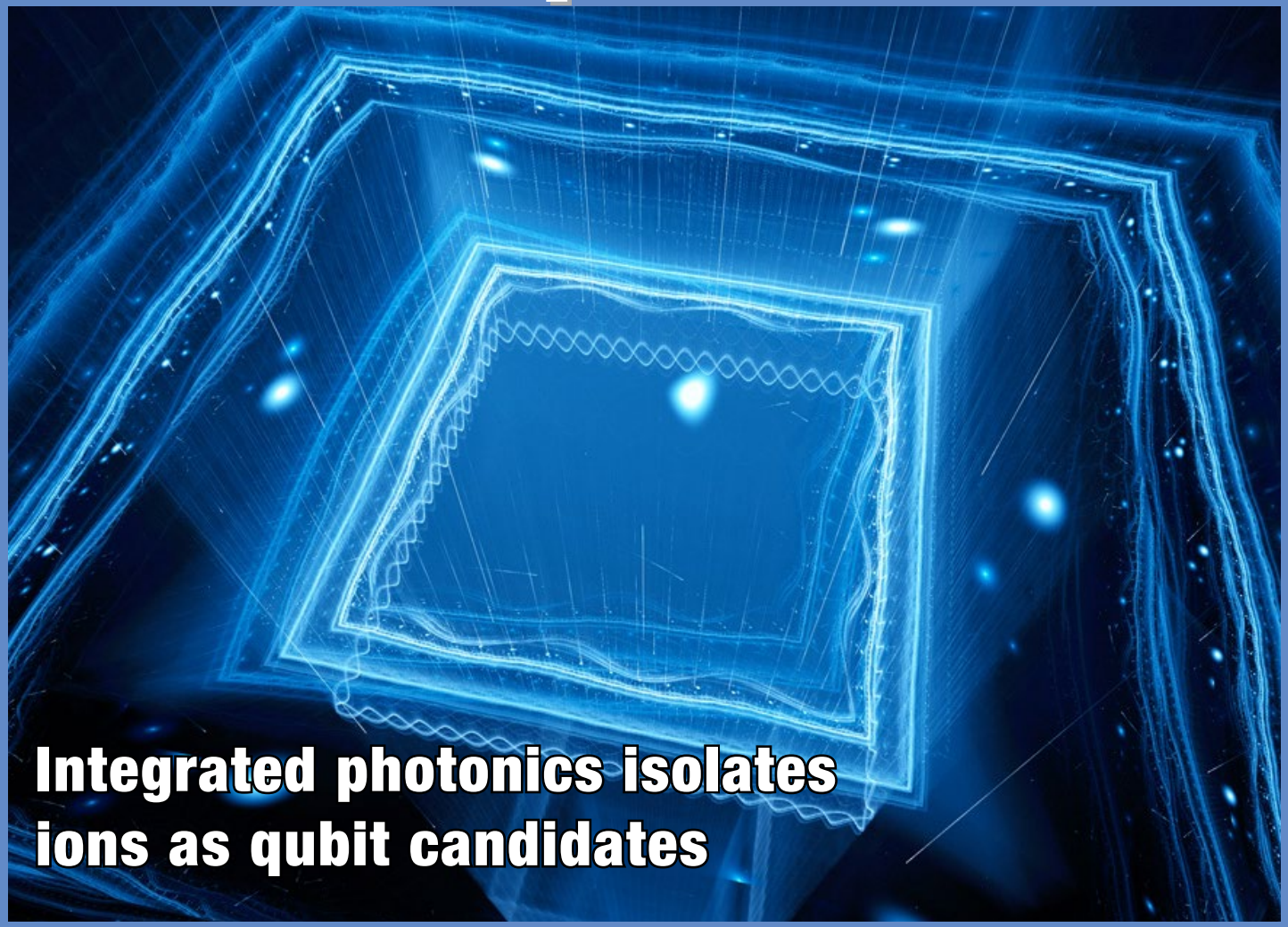
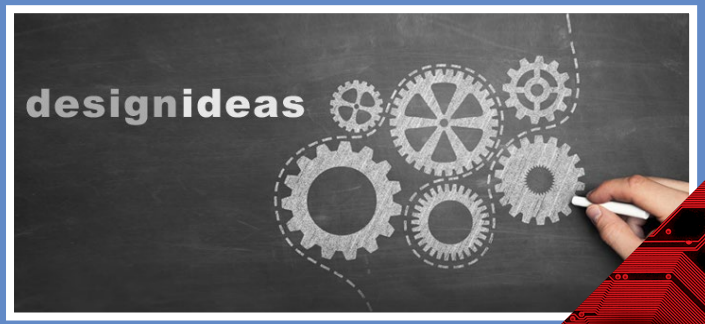


Integrated photonics isolates ions as qubit candidates



COVER

Integrated photonics offer a possible path to practical quantum computers

This month's cover image is a graphic created by MIT to accompany a news item on work done towards the eventual practical realisation of quantum computing. Using nano-scale semiconductor fabrication techniques to construct integrated optics could enable chips that use trapped ions as quantum bits. The work centres around applying integrated photonics – the combination of nano-scale electronic circuitry and optical waveguides – to the task of confining and observing ions whose quantum states are the basis of the qubit. Although quantum systems with as many as 12 qubits have been demonstrated in laboratory conditions, a fully practical quantum computer will require the handling of qubits to be "tamed" into a manageable and repeatable form of technology; or, as the MIT statement puts it; "... will require miniaturizing qubit technology, much the way the miniaturization of transistors enabled modern computers." Trapped ions are probably the most widely studied qubit technology, but they've historically required a large and complex hardware apparatus. Researchers from MIT and MIT Lincoln Laboratory describe work that promises a potential route toward practical quantum computers. Their paper describing a prototype chip that can trap ions in an electric field and, with built-in optics, direct laser light toward each of them. Full story here.

FEATUREARTICLES

ONLINE THIS MONTH

Where zero IF wins: 50% smaller PCB footprint at 1/3 the cost - Part 1, and;

Where Zero IF wins: 50% smaller PCB footprint at 1/3 the cost, Part 2

RF design in the 21st century

Making fog computing sensors clearly reliable

EDN's columns

GOOGLE ENDS ARA

Early in September, the Reuters news agency disclosed that Google had closed down its Ara project. Ara was the attempt to build a modular smartphone. The concept was that you (the user) would have a series of separate but communicating functional elements that you could slot together in the combination of your choice to add or subtract features depending on your needs at any given time. For example, you might choose to have a bigger battery; or a different display (sources mentioned an e-paper as opposed to an LCD or OLED panel); or an extra camera.

Such a platform could literally be all things to all people; configuration decisions on matters such as the balance between features and power demand/battery life – or size and weight – could be devolved from the design lab to the consumer. Also, the base platform could potentially support extended features, yet to be defined, in the future. Commentators who had been treated to an early view describe a prototype that looked not unlike a child's sliding-tile puzzle: rectangular blocks of variable size that fitted together into a superficially-conventional rectangle.

Any engineer who has struggled with the electromechanical will immediately see some of the inherent challenges in creating such a concept. The aesthetics of the format will depend on having the "tiles" join together with a satisfying "click" that must be maintained over many cycles – a mechanism that "clicked" and "un-clicked" a limited number of times, then "clicked" and came apart of its own volition, would only be a liability. Such mechanisms are not easily devised, nor is it easy to verify that they will survive and perform in the hands (or the jeans-pockets, or the handbags) of consumers.

Then, there is the matter of interconnect. Connectors can be the weakest point – as regards survivability and reliability – of many a design. One of the wonders of the age has been the surprising robustness of the ubiquitous micro-USB format – but the modules of a smartphone would need connectivity of a very different order, at least between some of its functional blocks. Those with deep R&D-budget pockets might consider a wireless link between modules; there's so much silicon in the design anyway, why not? A question that might be immediately countered with; power.

A modular design, by definition, creates a multiplicity of interfaces, some of which will be new and some of which will be buses that would be employed in a conventional design but now need to be pinned-out off-chip, or routed over longer distances and through interconnects. Moving data takes power; storing bytes, fetching bytes, driving lines – all are battery-sapping.

The latest reports confirm that the project has been wound up. Google appears to have recognised that this was a concept that wasn't going anywhere, and was unlikely to yield a marketable product any time soon. Google, we must assume, got to that most difficult review stage where faith in the concept has be balanced against progress (and money spent) to date, and the likelihood of reaching a satisfactory conclusion. The functionality vs. power equation may have looked too challenging: or marketing may have concluded that the increasing performance, in all dimensions, of the conventional smartphone simply didn't present a market "window" for a modular product. As outsiders, we will never know.

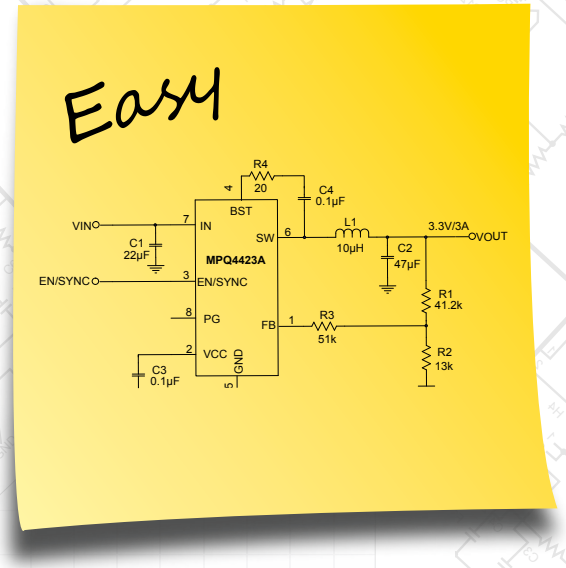
Google has the scale to put what it has learned into its cabinet of technology tricks, that it might draw on another day, and to move on. For a lesser company, this might be a matter of survival. But the project management process is the same at all scales – when the going gets tough, when do you persevere, when do you "keep the faith" with the project: and when do you close a project down and work on something else? The process is as much a part of engineering as anything done in the microamps, MHz and decibels domains.

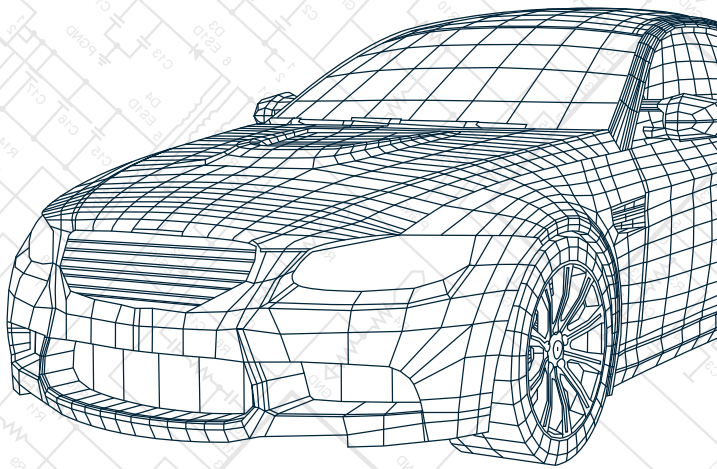
Simple, Easy Solutions

Design 101: Use MPS

MPQ4423A

Excellent Efficiency, 3A, 36V Synchronous Step-Down Converter





Key Highlights

- AEC-Q100 Qualified
- Wide 4V to 36V Continuous Operating Input Range
- 95% Efficiency Synchronous Mode Operation
- Good EMI, Compliant with CISPR25 Class 5
- Low Dropout Voltage for Automotive Cold Crank

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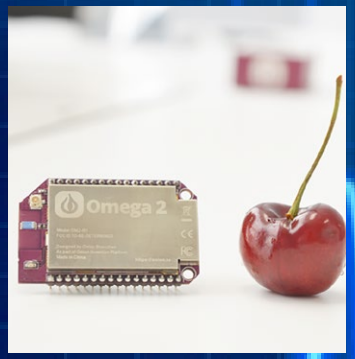
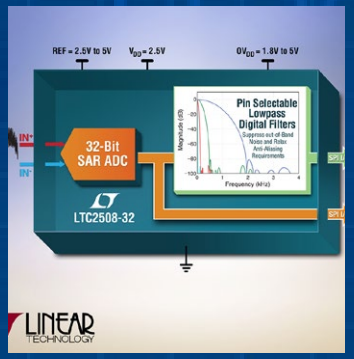
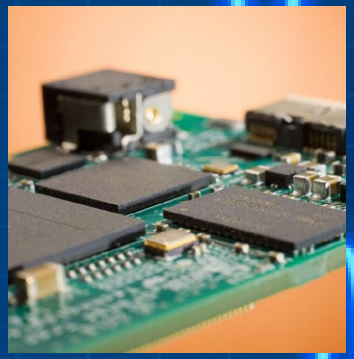
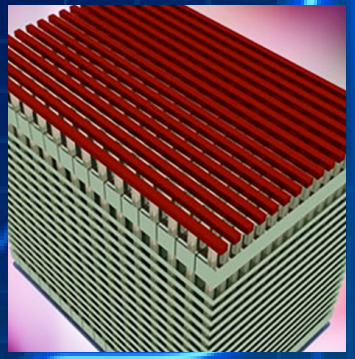

Omega 2


REF = 2.5V to 5V
V_{DD} = 2.5V
OV_{DD} = 1.8V to 5V
32-Bit
SAR ADC
LTC2508-32
Pin Selectable
Lowpass
Digital Filters
LINEAR
TECHNOLOGY






CleO 35


PREMIUM
MultiSIM BLUE
Mouser Professional Edition, Powered by National Instruments


muRata
20
30
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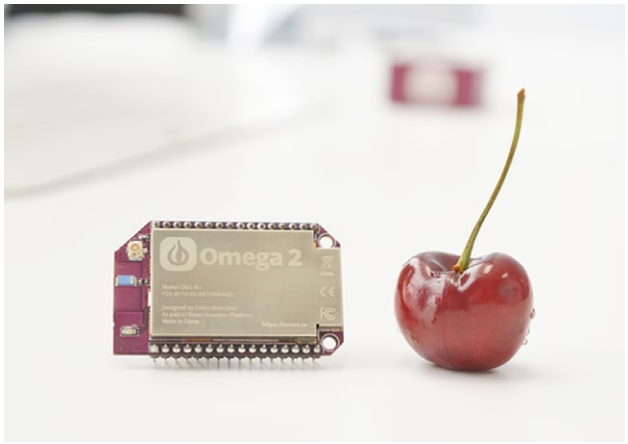
muRata
UMAL

$5 Linux + Wifi tiny IoT compute module completes crowdfunding

Omega 2 is a Linux compute module designed specifically for building connected hardware applications. It combines, say its designers Onion, "the tiny form factor and power-efficiency of the Arduino, with the power and flexibilities of the Raspberry Pi."

Omega 2 development was the subject of a Kickstarter campaign, that closed on August 23rd 2016 (here). The projects starts with the base module, which is an SoC-based board with built-in WiFi, and extends through levels of added connectivity, and peripherals – for example, there is a 'dock' card that provides compatibility with Arduino-format hardware. Part of Onion's offering is a cloud service, so that an Omega 2-based project can be fully cloud-connected and -enabled.



The chipset is the MediaTek MT7688, which uses a MIPS 24K core. Specifically, a 580 MHz MIPS 24KEc CPU with 64 KB I-Cache and 32 KB D-Cache. The SoC includes the 802.11n WiFi among numerous other peripheral functions. Omega 2 (the one with the base price of $5) includes 64 MB of memory and 16 MB of storage; the $9 Omega 2 Plus ups this to 128/232 MB and adds an SD card slot. Both have USB 2.0, 15 GPIOs, 2 PWM and 2 UART channels, I²C, SPI and I²S.

There is already a range of third-party add-ons, for example a company called Hologram has a cellular radio expansion car, itself based around a u-blox radio module.

Complete article, here

Where is the worldwide semiconductor industry headed?

The market analysis firm Future Horizons will need no introduction for any long-term followers of the fortunes of the semiconductor industry. Headed by Malcom Penn, its reports and seminars have tracked and predicted the fortunes of the sector over many years. Next up in that continuing series is Future Horizons' IFS2016 Mid-Term Semiconductor Market Outlook & Forecast.

This is a one-day presentation which will take place on Tuesday, 20th September 2016, in London. As always, Malcolm and colleagues will take stock of the recent performance of the industry, and will look ahead to what is likely to shape the coming months, quarters and beyond; and will project how the environment will look for the chipmakers themselves; for their customers; and for suppliers to the semiconductor business.

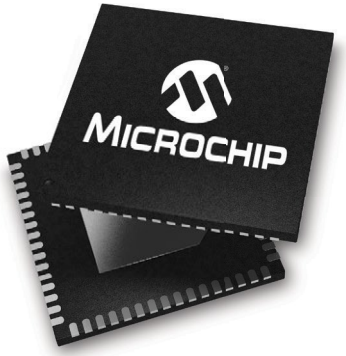
This will the first such analysis since the UK's vote to leave the EU; while that many have only a limited direct impact on semiconductor industry turnover, it may be seen as contributing to the climate of uncertainty and minimal growth that characterises Eurozone and associated economies. Future Horizons notes other political – or quasi-political – factors such as, "Traditionally the chip market grows strongly in a US presidential election year but 2016 seems likely to follow 2015's no-growth performance. For the industry to thrive, it needs a strong and stable economy, something that has eluded the market since the 2007-8 financial crises. Economic

First PIC32 MCUs with Core Independent Peripherals

Overcoming cost, power and size limitations with PIC32MM MCUs

As the first PIC32 microcontrollers to offer Core Independent Peripherals, the PIC32MM family delivers cost-effective, low-power embedded control for IoT, consumer, industrial and sensorless BLDC applications.

The Core Independent Peripherals, such as configurable logic cells (CLC) and multiple-output capture compare PWMs (MCCPs), off-load tasks from the CPU to deliver lower power consumption and lower design complexity. Further power savings, from low-power sleep modes, are combined with small, 4x4mm package options to support longer battery life even in space-constrained applications.



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uncertainty continues to dampen business confidence. Bad in itself, in times of uncertainty firms delay new investment, do not hire staff and push out decision making … all of which has an adverse impact on the semiconductor market."

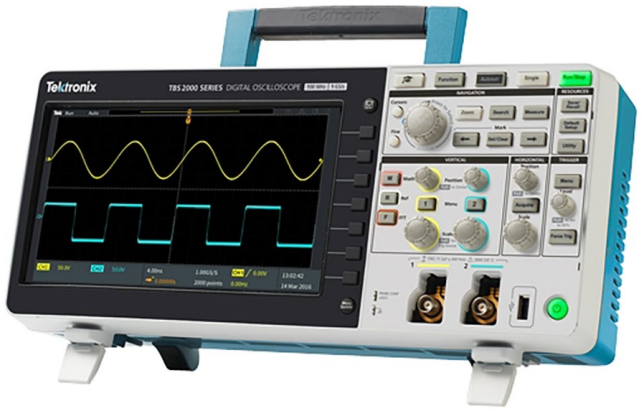
The day-long seminar will consider the technologies and design trends that will come to bear in the near-term; will the Internet of Things be a source of new growth? "What too of the impact of the new, platform-centric vertical end-markets? We saw the impact this had on the mobile market … will automotive - the world's biggest potential IoT market - be the next area for attack? What too of Robotics and the impact of deep-learning, both from a chip market prospective and economic tipping point?"

Complete article, here

Tek renews basic troubleshooting/education scope line, from €1,140

Tektronix says its TDS2000 series is the most widely-used scope in the world: now, it has introduced a completely new product in that space, for basic lab signal viewing, and for education – the TBS2000. It offers, Tek says, the best signal viewing in its class, with a 9-inch, widescreen-format LCD and the longest record length in this market sector.

Models are available with 70 MHz or 100 MHz bandwidth and with 2 or 4 channels. The instrument's design exploits the widespread availability of high-quality, 16 x 9 format LCD to offer a WVGA display that can display 15 horizontal (time) divisions allowing users to see 50% more signal than any other scope in this category. Long record length is only valuable if signals can easily be manipulated to find events in the record; this instrument's 20 Mpoint record length together with single-knob pan and zoom provides the ability to capture long time duration signals and easily navigate to find important details.



Triggering borrows from higher-priced ranges, with a range of edge, pulse-width and 'runt' (anomalous level) trigger settings. A basic FFT function is also included. Interfacing allows connection to WiFi via USB; and for use in an LXI environment, the scope generates a web page. Interfaces, like many other features of the scope, are aimed at education users.

Isolated 1-GHz b/w probing system shipping

Tektronix' IsoVu optically isolated measurement system has been "soft launched" with demonstrations at various trade shows in 2016; now, Tek has announced it is delivering the systems which provides 1 GHz bandwidth, wide common mode range, and very high common mode rejection to make previously hidden signals visible. We first covered the IsoVu system in March 2016 and reported its appearance at the PCIM show, 2016. Tek is now shipping the system, with pricing that starts at $12,000 (more on pricing in the full item, here).

The IsoVu platform uses an electro-optic sensor to convert input signals to optical modulation, electrically isolating the device-under-test from a Tektronix oscilloscope. The system incorporates four separate lasers, an optical sensor, five optical fibres, and sophisticated feedback and con-

trol techniques. The sensor head, which connects to the test point, has complete electrical isolation and is powered over one of the optical fibres.

A critical advantage this technology offers for designers, such as those working on power devices involving GaN and SiC technologies, is superior common mode rejection that makes signals previously buried in common mode noise visible for the first time.

IsoVu offers 1 million:1 (120 dB) common mode rejection (CMRR) up to 100 MHz and 10,000:1 (80 dB) CMRR at 1 GHz. Tektronix says, "Currently there is no measurement system on the market with IsoVu's combination of high bandwidth, 2000V common mode voltage range and breakthrough common mode rejection ratio."

The exemplar application that Tek cites is that of observing detailed switching behaviour of the power semiconductor device in, say, a high-power inverter, where millivolt-scale waveforms are of interest but they are "on top of" a voltage level of several hundred Volts. As well as being able to make such measurements, IsoVu brings a major safety benefit with total isolation of the measurement system from the system under test; with the optical fibre links, the oscilloscope (and the engineer) can be outside a fully-screened enclosure when needed.

Complete article, here

Hardened OS turns Raspberry Pi into VPN gateway and firewall

By Julien Happich

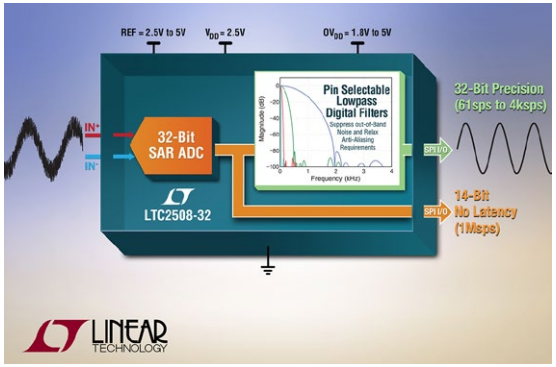
Infotecs has developed a cost-effective cyber security solution based on Raspberry Pi, turning the credit card-sized mini-PC into a fully-functional VPN gateway and firewall based on ViPNet technology.

The solution for the Raspberry 3 model B consists of a hardened Linux-based operating system and ViPNet Coordinator. In combination with Raspberry Pi, the image forms a hardware appliance. The solution provides highly secure protection against both external and internal threats – at a reasonable price. It may also be implemented to encrypt networked computer cash register systems in retail, or protect VoIP, printers, building infrastructures, and IP video cameras. Another example of an area which can benefit from the solution is telecommunications, where Infotecs enabled secure Raspberry Pi can provide secure and cost-efficient systems access.

Complete article, here

32-bit SAR ADC, digitally filtered, 1Msps, 0-latency outputs

LTC2508-32 is an ultrahigh precision 32-bit successive approximation register (SAR) analogue-to-digital converter (ADC) for high performance applications, including data acquisition, industrial control and medical instrumentation, requiring both accuracy and speed.
This is often achieved by using a high resolution delta-sigma ADC and a high speed SAR ADC in the same system. The LTC2508-32 simplifies such hybrid ADC system design by simultaneously providing both a 32-bit low noise digitally filtered output and a 14-bit 1 Msample/sec no-latency output. Since these outputs are generated from a single 32-bit SAR ADC core, the high accuracy and high speed outputs are matched, even as the operating temperature, supply and stress vary. In contrast to traditional solutions employing two distinct unmatched ADCs, the combination of both accuracy and speed in the LTC2508-32 enables much higher system performance while reducing solution size and lowering component count.



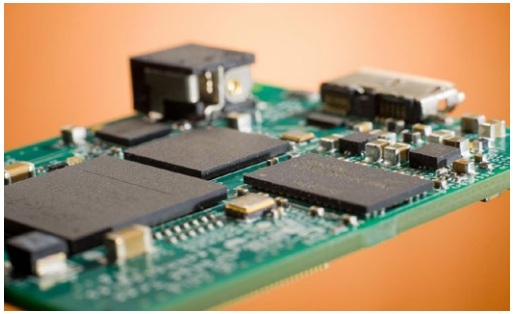
The LTC2508-32 is suitable for applications that simultaneously require precision measurement and fast tracking of signals. The 3.5 ppm guaranteed maximum linearity, together with up to 145 dB of dynamic range, enables the LTC2508-32 to make precision measurements in the presence of noise. Simultaneously, the high speed 1 Msample/sec output provides a 14-bit differential and 8-bit common mode representation of the input signal, enabling sophisticated control loop designs with early detection mechanisms. The LTC2508-32 further improves system accuracy while simplifying signal conditioning design by directly digitizing the input signal over the full input range with over 120 dB of common mode rejection. The LTC2508-32 features an integrated digital filter that can be configured to optimize the 32-bit high accuracy output's noise performance and bandwidth, up to a maximum 145 dB of dynamic range at an output data rate of 61 sample/sec.

Complete article, here

USB 3.0 FPGA module sustains 360 MB/sec data transfers

By Julien Happich

Orange Tree Technologies has released the ZestSC3, an FPGA module built around Xilinx' Artix-7 user-programmable FPGA and a very high performance SuperSpeed USB 3.0 interface.
The new module provides a simple, easy to use way to transfer large amounts of data quickly between a computer and the outside world, without having to integrate complex hardware and software. The ZestSC3's USB 3.0 interface can sustain 360 MB/sec of data transfer in either direction, enabling new, bandwidth hungry applications. Measuring 40 x 50mm, the module is suited to integration in embedded systems and OEM equipment. 105 user I/O pins provide maximum flexibility for end applications.
The user-programmable Xilinx



Artix-7 FPGA is coupled with 512 MB of high speed 1.6 GB/sec DDR3 memory. The FPGA can be programmed from the 8 MB of on-board Flash, USB or JTAG. It can be used as a programmable interface to external devices, for high speed processing of streaming data, and for data acquisition and control.
The module can be used as a stand-alone board powered over USB, and includes the ability to program the user FPGA and Flash over USB without requiring additional programming cables or hardware. Flash can also be used for user data storage. Requiring only a single 3.3V-5V power supply, the new module is simple to integrate into a larger system.

Complete article, here

LoRaWAN development kit leads to faster IoT projects

Semtech has announced that two European members of the LoRa Alliance have jointly released a development kit for IoT projects. Libelium (Spain) and Loriot (Switzerland) created the kit to make it easier to develop smart city, smart security, smart environment and smart agriculture applications. Comprising a gateway and ten sensor devices, and employing Semtech LoRa technology, application software, and a connection to Loriot's cloud-based LoRaWAN network, the kit is intended for smart city, smart security, smart environment and smart agriculture applications. The kit is available for both North America (915 MHz) and European (868 MHz) frequencies.

Javier Martínez, Libelium's Vice President of Business Development & Sales comments,"With our kit, customers do not have to spend time configuring and testing a network, because we are able to provide them with a LoRaWAN network connection that has already been tested and set up to run seamlessly with the kit components and software."
Semtech, Libelium, and Loriot are members of the LoRa Alliance, a group of over 300 companies committed to driving and enhancing the LoRaWAN specification to ensure interoperability and scalability of LPWANs and IoT applications. The Alliance claims that there are LoRaWAN public and private networks in more than 50 countries worldwide.

Complete article, here

mmWave expertise takes Rohde & Schwarz into security body scanners

Readers of these pages will know Rohde & Schwarz for its test and measurement instrumentation (and broadcast/communications product lines, among others). Now, employing that experience in a different direction, the company has won a significant order from the German government for millimetre-wave security body scanners, for use at airports and and other checkpoints.
In July 2016, the Procurement Office of the German Federal Ministry of the Interior signed a framework agreement with Rohde & Schwarz for 300 R&S QPS200 security scanners, over a 3-year period. The instruments can be now be used everywhere that the

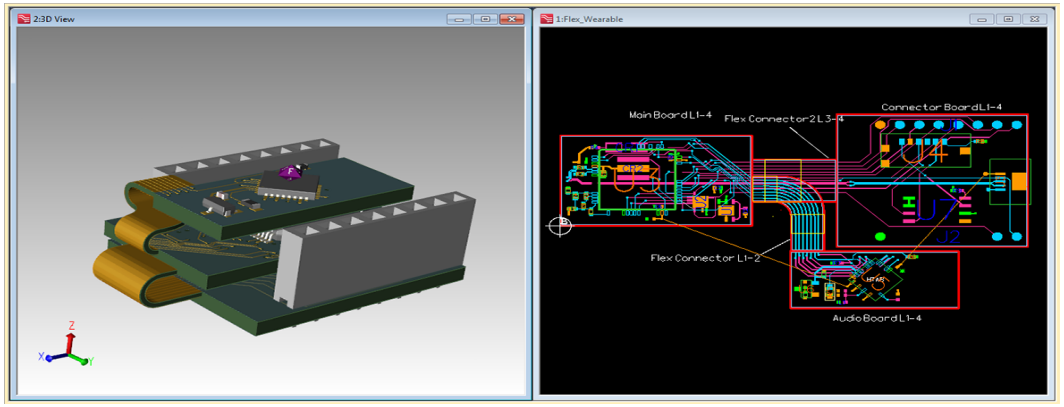
German Federal Police Force performs security checks. The primary application will be for security at German airports.
The R&S QPS200 becomes the preferred selection for the Federal Police for security checks at airports throughout Germany. The scanners can also be used for security access control in other places, such as in ministries, for example. The security scanner automatically detects potentially dangerous objects under clothing or on the body, whether they

are rigid, flexible, fluid, metallic or non-metallic. If the scanner reports an alarm, the location of the object is marked on an avatar, a symbolic graphic of the human body.
The scanner employs a fixed array of "thousands of transmitters and receivers" and the design has no moving parts, unlike existing designs in which the subject must remain still while a linear array is rotated around them. It permits an open design which improves visibility and allows wheelchair access, also eliminating the "claustrophobic", closed-cabinet aspect of prior designs.
R&S notes that there "is no health hazard associated with the R&S QPS transmit power", (the specification says a power of 1 mW) which is "hundreds or even thousands of times lower than that of a mobile phone". It operates in the frequency range between 70 GHz and 80 GHz. A scan takes 32 milliseconds to complete.

Complete article, here

Mentor extends rigid-flex & high-speed PCB design in Xpedition

Mentor Graphics has announced the first phase of its Xpedition printed circuit design flow to address the increasing complexity of today's advanced systems designs. The Xpedition flow provides advanced technologies to enable design and verification of 3D rigid-flex structures, and to automate layout of high-speed topologies with advanced constraints.
Flex and rigid-flex PCBs, Mentor comments, are now found in all types of electronics products, from small consumer devices to aerospace, defence and automotive electronics. The Xpedition rigid-flex technology enables a streamlined design process from initial stack-up creation through manufacturing.



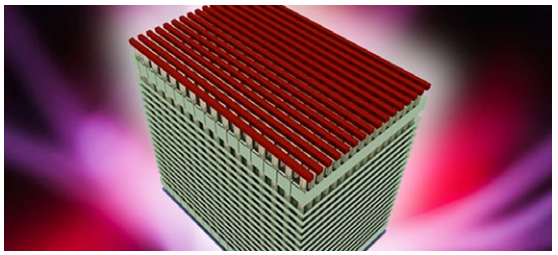
Engineers can design complex rigid and flex PCBs in a fully supported 3D environment (3D design and verification—not just a 3D view), resulting in a correct-by-construction methodology for optimum reliability and product quality. 3D verification ensures that bends are in the right position, and elements on the board do not

interfere with folding; this can be reviewed early in the design stage to prevent costly redesigns. Users can then export a 3D solid model to MCAD for efficient bi-directional PCB-enclosure co-design. Integration with Mentor's HyperLynx high-speed analysis technology enables optimization of signal and power integrity across complex rigid-flex stack-up structures. For fabrication preparation, the Xpedition flow provides all flex and rigid information using the ODB++ common data format. This methodology eliminates data ambiguities by clearly communicating the finished board intent to the fabricator.

Complete article, here

Toshiba starts sampling of 64-layer 3D flash memory at 256 Gbit density

Toshiba Corporation has disclosed the latest generation of its BiCS FLASH three-dimensional (3D) flash memory with a stacked cell structure, a 64-layer device that it claims as the first to start sample shipments.
The new device incorporates 3-bit-per-cell (triple-level cell, TLC) technology and achieves a 256-gigabit (32 gigabytes) capacity, an advance that underscores the potential of Toshiba's proprietary architecture. Toshiba continues to refine BiCS FLASH, and the next milestone on the development roadmap is a 512-gigabit (64-gigabytes) device, also with 64 layers.

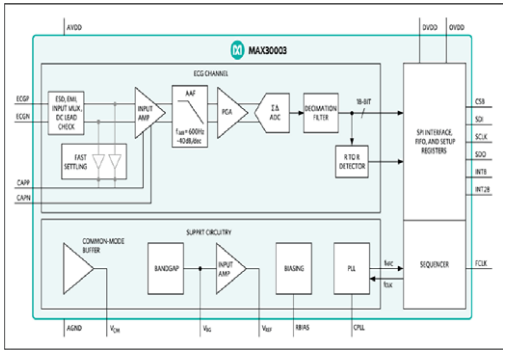


The new device succeeds the 48-layer BiCS FLASH [to which the above graphic relates], and its 64-layer stacking process realizes a 40% larger capacity per unit chip size than 48-layer stacking process, reduces the cost per bit, and increases the manufacturability of memory capacity per silicon wafer. 64-layer BiCS FLASH can meet demanding performance specs, and the new device will be used in applications that include enterprise and consumer SSD, smartphones, tablets and memory cards.

Complete article, here

Ultra-low power 85microwatt, integrated biopotential AFE

Maxim Integrated has posted preliminary information on its MAX30003, which is a complete, biopotential, analogue front-end solution for wearable, clinical and fitness applications, with ultra-low power for long battery life. The MAX30003 is a single biopotential channel providing ECG waveforms and heart rate detection.
The biopotential channel has ESD protection, EMI filtering, internal lead biasing, DC leads-off detection, ultra-low power leads-on detection during standby mode, and calibration voltages for built-in self-test. Soft power-up sequencing ensures no large transients are injected into the electrodes. The biopotential channel also has high input impedance, low noise, high CMRR, programmable gain, various low-pass and high-pass filter options, and a high-resolution



analogue-to-digital converter. The

biopotential channel is DC coupled, can handle large electrode voltage offsets, and has a fast recovery mode to quickly recover from overdrive conditions, such as defibrillation and electrosurgery. It comes in a 28-pin TQFN and 30-bump wafer-level package (WLP), operating over the 0°C to +70°C commercial temperature range.

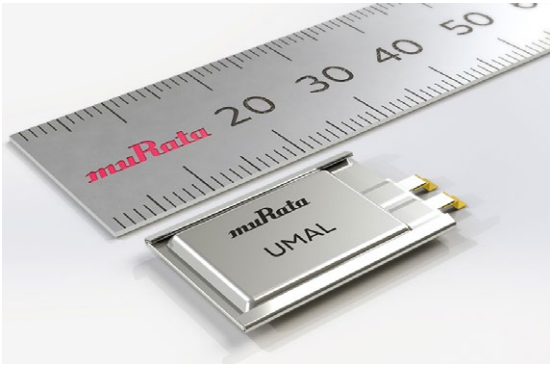
Use the device, Maxim suggests, in bio-authentication and ECG-on-demand applications; chest band heart rate monitors for fitness applications; single lead event monitors for arrhythmia detection; and single lead wireless patches for at-home/in-hospital monitoring.

Complete article, here

Not a battery or a supercap, but a thin laminate energy device

Murata's UMAL is a low-profile high capacity energy device. Designed to meet the demand for a slim high capacity energy source with a maintenance-free extended life cycle in wireless sensor nodes, the UMAL has charge/discharge and life-cycle characteristics superior to conventional secondary batteries.

The UMAL has a nominal voltage of 2.3 VDC, can supply 12 mAh with a maximum discharge current of 120 mA and is able to withstand load fluctuations. It has a low internal resistance of 200 mOhm and can operate over the temperature range of – 20C to + 70C.



The nominal charge voltage is 2.7 VDC and the UMAL is capable of fast charging / discharge. In particular the device's high-rate discharge characteristics mean that a peak-assist capacitor is not required. It also has a charge capacity recovery rate of over 90% after 5,000 charge / discharge cycles. The UMAL measures 2.0 x 14.0 x 21.0 mm.

The device has a chemically stable composition that does not cause a fire or smoke hazard even if the output terminals are shorted. In addition to wireless sensor nodes, the UMAL is also suitable for use in wearable designs.

Complete article, here

3D printing tool is all-in-one pen, precision solder, burner, and cutter

Amy Norcross

A refined, "smarter" version of the 3DSimo product that was released by the Czech company of the same name in October 2013, the much smaller 3DSimo Mini builds on the capabilities of the original 3DSimo as well as the capabilities of the world's first 3D pen, the 3Doodler, which Engadget's Brian Heater described as "a bit like a hot glue gun for plastic — simple and ingenious."

The 3DSimo also presses melted/quickly cooling plastic out of a die. It distinguishes itself, however, with added functionality.

"We created the 3DSimo Mini to be the ultimate creator's tool,"

says David Paskevic, CEO of 3DSimo. “It is more than a 3D printing pen. Immediate uses include extensions for burning, foam cutting, and soldering. In the future, we will incorporate additional functionality to the pen, such as drilling, making it a practical tool for creators of any skill set. The Mini is a tool that can be used for all creative projects.”

Able to fit in the palm of your hand and provided with several changeable tips, the 3DSimo Mini allows you to 3D print using one of close to a dozen different materials as well as solder, burn, and cut foam. Housed in an ergonomic, user-friendly white case that measure 163×36×22 mm and weighs 40 grams, the tool offers changeable tips and turns an “ordinary” 3D printing pen into a multipurpose tool for 3D drawing, soldering, burning, and cutting. It features an LED display and can reach a temperature of 490 degrees Celsius at the tip. The 3DSimo Mini accepts spools of 1.75-mm filament, such as ABS, HIPS, PLA, and Thermochrome. Users can create models that glow in the dark or that change colour based on temperature fluctuations.

Complete article, here

Arduino-compatible touch-enabled display shield from FTDI

CleO is a simple to program, intelligent TFT display solution that allows the construction of human machine interfaces (HMIs) with – says maker FTDI chip – much higher performance than conventional Arduino display shields are able to deliver.

FTDI says that engineers of all different levels of aptitude (from seasoned professionals right through to keen amateurs) can develop next generation HMIs exhibiting high levels of functionality and superior graphical qualities. The initial CleO offering comprises a HVGA resolution, 3.5-inch TFT display incorporating a resistive touchscreen and supporting both portrait and landscape implementations. An FTDI Chip FT810 high resolution embedded video engine (EVE) graphic controller executes the HMI operation, while one of the company’s 310DMIPs FT903 microcontrollers addresses all additional processing tasks. This display shield provides smooth animation of graphical content, even at 60 fps frame rates. Anti-aliased graphics capabilities render images in finer detail - eliminating the unwanted presence of jagged edges.

When CleO is combined with FTDI Chip’s NerO - an energy efficient Arduino-compatible design capable of operating up to 1W, FTDI asserts that it offers a far more powerful solution than a nor-

mal Arduino-format UNO/display shield package. However, its Arduino compatibility means it can also connect with the wide variety of different shields (sensors, motors, switches, etc.) available for this platform.
CleO has an array of accessories; with dimensions of 57.15 x 54.35 mm, the CleO-RIO module provides a mechanism for stacking the CleO shield and an Arduino board together. The CleO-Speaker module (which measures 63 x 63 x 23.8mm) facilitates the playback music/tones for HMIs where audio has been incorporated. There is also an audio line for input of audio from external sources. The CleO-Camera module has an OV5640 1/4-inch 5 Mpixel CMOS image sensor plus flash LEDs and a 24-pin 0.5mm pitch FFC cable. There is also a 9V power adaptor which provides the NerO/CleO solution with up to 1A of current.

Complete article, here

Mouser boosts circuit design software features with MultiSIM BLUE Premium

Distributor Mouser Electronics' MultiSIM BLUE Premium is the latest release of the Mouser Edition of the National Instruments Multisim circuit design tool. The premium edition, for €300 per licence, extends the (free version) MultiSIM BLUE design tool's abilities to capture, simulate, carry out PCB design, BOM export and purchase, and adds flexibility and functionality.
MultiSIM BLUE Premium offers unlimited components within the schematic and integrated design capabilities. The advanced tool provides engineers with a simulation environment using Mouser's selection of products and a larger selection of NI components, including the newest in analogue and mixed-signal ICs, passive components, discrete semiconductors, power management ICs, connectors, and electromechanical components.
Featuring an industry-standard Berkley SPICE simulation environment, MultiSIM BLUE Premium provides engineers with the freedom to design and simulate circuits before laying them out in physical prototypes. Engineers can now visualize and evaluate linear performance, making this critical step of circuit design easier, faster and far more productive.

Complete article, here

Nordic Semi sets sights on low power cellular IoT

Nordic Semiconductor has set out how it intends to expand its low-power radio product to make use of cellular services, including narrow-band IoT (NB-IoT) and the emerging 3GPP Release 13 LTE-M. Product will be designated as the nRF91 Series, to include highly integrated chipsets and software.

Not yet a product announcement, Nordic is flagging its development of a low power LTE technology for cellular Internet of Things (IoT). This development builds on Nordic's ultra low power (ULP) wireless capabilities and its recruitment of a group of cellular R&D engineers in Finland (formerly employed by the Finnish arms of Nokia, Ericsson, Motorola, and Broadcom).

Low power cellular IoT, Nordic comments, is being positioned to be widely adopted in numerous markets and applications including, for example, smart utility metering, asset and people (e.g. child) tracking, fleet management, buildings security and safety, remote maintenance, smart vending machines, retail, healthcare and medical monitoring, real-time traffic monitoring, wearables, indoor and outdoor GPS navigation, smart home technology, automotive (e.g. customized insurance based on actual driving data), and industrial and agricultural automation.

Nordic Semiconductor's roadmap for low power cellular IoT includes highly integrated chipsets and software for the forthcoming 3GPP Release 13 LTE-M and NB-IoT cellular technologies. Optimized for power and size, the forthcoming Nordic Semiconductor nRF91 Series is designed specifically to address the needs of emerging low power cellular IoT applications, including long battery life, low cost deployment and maintenance, scalability for potentially billions of devices, a miniaturized form-factor that can fit almost anywhere, and ubiquitous network coverage.

Nordic expects to sample the first nRF91 Series solutions to lead customers second half of 2017, with broad availability and production ramp following in 2018.

Complete article, here

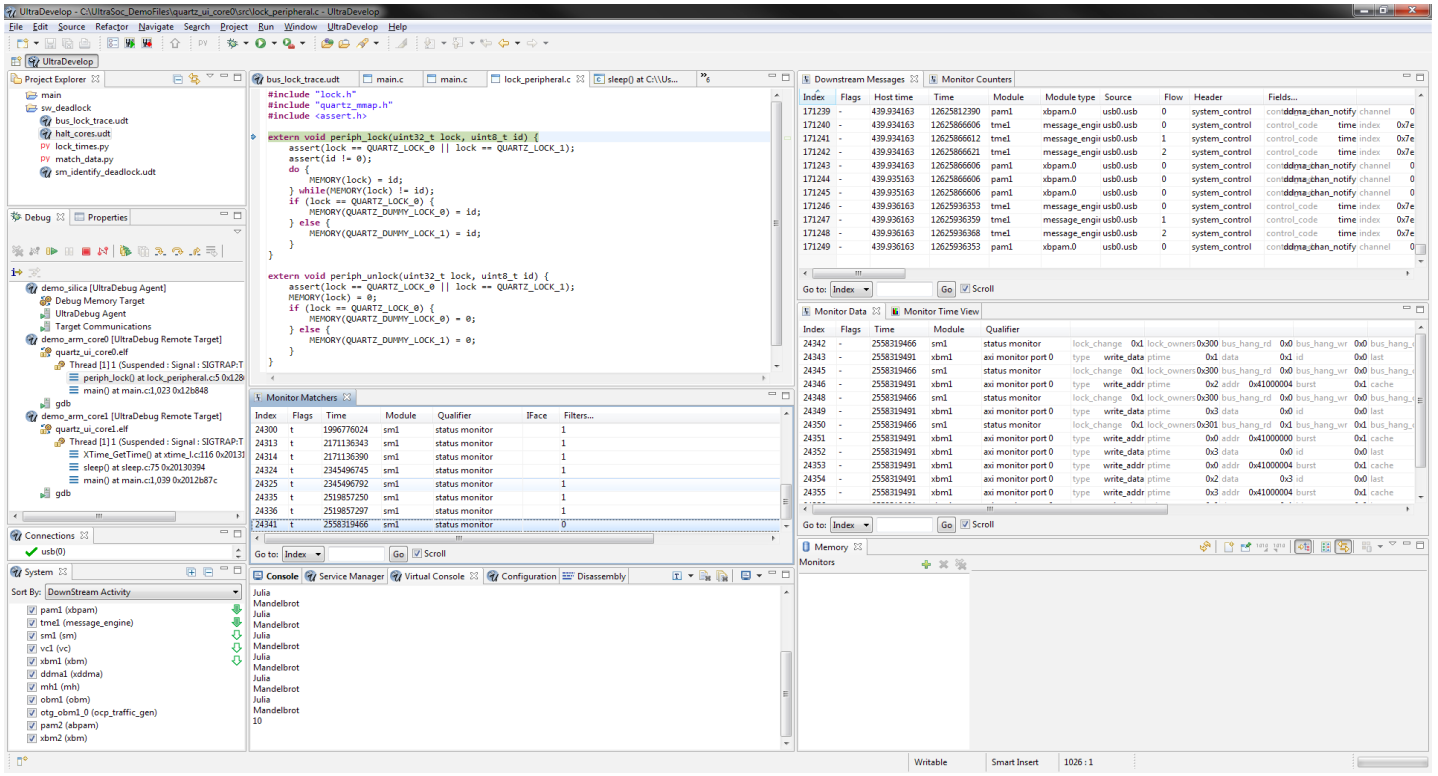
SOC DEBUG: THE NEED FOR VISIBILITY

By Gajinder Panesar, Ultrasoc

Debug is a crucial component in the successful development of any embedded system. Yet its efficient implementation is a component that is often overlooked because of the inherent difficulties that are encountered when it is implemented using traditional techniques.

Software now provides much of the functionality of a broad spectrum of devices and systems. Software quality – and the ways in which the software interacts with the hardware on which it runs – is therefore now of paramount importance. The failure to detect bugs until shortly before a product's launch deadline has been responsible for costly and embarrassing delays to companies, resulting in millions of dollars of lost revenue. The consequences for not detecting serious bugs until after launch can be even worse, leading to product liability lawsuits and the need for expensive recalls.

The situation has become even more difficult to deal with as the emphasis in embedded systems has shifted from uniprocessor systems – a paradigm for which most debuggers were originally designed – to a much more complex, often heterogeneous multiprocessor environment.



Debug requirements

The ideal debugger for systems and software verification provides a high degree of visibility and control. High visibility ensures that programmers and system architects can see how values are manipulated inside the SoC processing units and stored in memory: this real-life behaviour can then be compared to the engineering team's mental model of what should be happening. Write access to the target is important: it provides the developer with the ability to alter values in registers or memory to see the effect of changes without having to recompile code.

Control over the target is equally important. Target control stops and restarts the system deterministically. It is vital that other values are not updated before these changes are made. And breakpoints that stop the processor at a point in time based on conditions such as a variable going out of range or an address being hit need to be in place to stop the system and prevent it moving into an unpredictable state

from which it will be difficult to recover useful data.

In the SoC design environment, simulation has become an important platform for software development. The use of simulation for early development has a number of advantages and one fundamental disadvantage. A full complement of debug features is readily available under software-based simulation because the infrastructure around the model of the processor has full access to its state and internal signals. As the simulation provides access to a virtual target long before the availability of actual hardware, software teams can begin work very early in the project life cycle and explore aspects of the application design before features and functions are finally decided.

With ready access to the (simulated) internal state of the processor, the programmer can easily trace through the execution of a critical section of code using single-step functions and work backwards through a sequence to trace an erroneous result to its source.

Unfortunately, simulation is orders of magnitude slower than the target hardware. This often means that only a small proportion of the overall application code can be tested on the simulated hardware. Emulation and simulation acceleration improve the performance of the virtual target. But depending on the platform, the impact on debug visibility can be minimal. Emulation platforms based on custom SoCs have been refined to the point where they can support the streaming of many internal logic signals to a visualization workstation that can be used to support software debug.

The fastest prototyping platforms are generally based on boards carrying multiple field-programmable gate arrays (FPGAs) that are intended to function together as a virtual SoC. But the higher performance comes at a cost. First, it takes longer to put the virtual target into the FPGA fabric than it does to compile a hardware design for emulation. Second, these FPGA prototyping systems greatly restrict the number of internal logic signals that can be passed to the outside. The only signals with guaranteed access are those that will be used by the final SoC to communicate with its environment.

FPGA prototyping platforms allow for some degree of internal logic capture but the introduction of internal probe points to route logic signals out of the device often has a significant impact on performance. The slowdown can be a factor of ten or more, which reduces the advantage of using the FPGA prototype over an emulator when it comes to execution speed.

The greatest execution performance is available when the SoC arrives from the fab and has passed its initial qualification tests and is running on prototype PCBs. But at this point, unless provisions have been made, internal visibility is highly limited.

Debug access

Until the 2000s, debug visibility for embedded processors was improved primarily through bondout packaging of a processor assisted by the traces provided by logic analyzers to identify issues with communication to off-chip peripherals. But this gave way to other debug techniques and increasing integration meant that the ability to use logic analyzer probes vanished.

The author continues this article by looking at the various schemes that have been applied to improve visibility of internal SoC operation; and outlines an approach appropriate to complex multicore devices. Click for pdf.

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STATISTICAL PROFILING AIDS CODE UNDERSTANDING

BY JACOB BENINGO

The second the Run button is pressed on the IDE, the microcontroller begins executing millions of instructions a second. But what functions are executing and how often? How much time is spent idling the processor vs code execution? Nobody knows! Statistical profiling can help answer these basic questions.

For years, engineers could only guess at how their code was actually executing or, when forced to, instrumented their code with complex and time-consuming setups to answer basic and fundamental system questions. Happily, engineers today can use statistical profiling to find the answers. Statistical profiling is a method for estimating which functions are executing on the microcontroller and what their load is on the processor. (An example video that walks through the setup for statistical profiling can be found here.)

Modern 32-bit architectures, such as the ARM Cortex-M, contain a mechanism known as the Serial Wire Viewer (SWV) for sending such information over the Serial Wire Debugger. The debug hardware has the ability to periodically sample the Program Counter (PC) register and transmit its value over the debug probe to the host development environment. The host can then take the PC value and correlate it with the line of code, and therefore the function, that is being executed. Sampling the PC at a fairly rapid rate allows the host to gather the application's basic statistical profiles, such as the function being executed and how much time is spent executing the function.

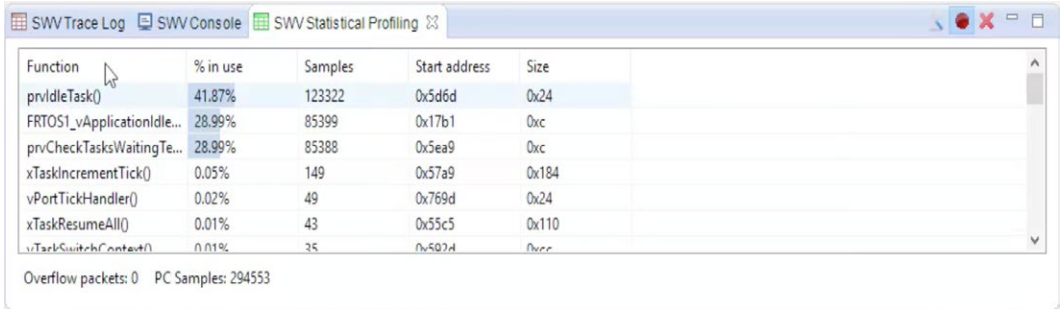


Figure 1. *Statistical profiling*

Armed with statistical profiling information, a developer can now understand how much CPU time is being dedicated to a given function. Not only does profiling this provide insights into how the code is executing, it can point a developer toward potential problems and areas that may require optimization. Embedded systems that are using an RTOS can even check to see how often the idle task is being called, which provides information related to how loaded the CPU is.
An example statistical profile can be seen in Figure 1. In this case, an RTOS with three tasks that blink LEDs is executing. The CPU is spending over 70% of the time in functions related to executing the idle tasks which means the CPU is nowhere near capacity.

Setting up statistical profiling is relatively straight forward but may vary based on the development environment being used. The processes will be similar but the details and nuances may vary slightly. As an example, let's look how to setup statistical profiling using the free Atollic TrueSTUDIO. The first step to set up the profiler is to enable SWD trace and set the Baud rate for the data. In TrueSTUDIO, and most Eclipse based IDEs, this setup can be done by accessing the Debugger tab within the debug configuration. A developer will find configuration settings similar to those in Figure 2. The developer must set the trace option to SWV (Serial Wire Viewer) and then also set the core clock frequency. The profiler will return PC

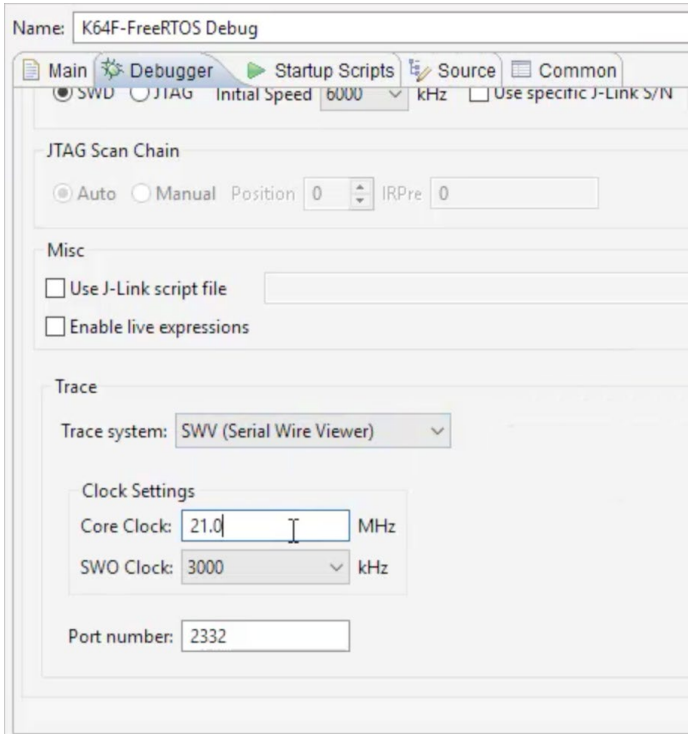


Figure 2. *Enabling system trace capabilities*

values to the debugger at a rate proportional to the core clock frequency. Because the communication is serial, if the debugger doesn't know the data rate the received data cannot be properly interpreted. The result: profiling will not work.

Once the core clock frequency has been set, developers can save the updated debug configuration and initiate the debug session. When the target has been loaded with the test code, developers can access a Serial Wire Viewer settings menu to bring up the settings. In order to perform profiling, disable any other debug options available and only enable the PC Sampling option, as shown in Figure 3.

The rate at which the PC register is sampled is adjustable by means of the SWD clock rate. If the PC is sampled too quickly, packets can be lost. On the other hand, if the PC is not sampled fast enough not every function that is executed may show up in the profiler. The odds of catching the PC in short functions is very small if the sample rate is low. So, be careful selecting the SWD clock values!

Once the PC Sampling option has been configured, a developer can commit the changes, press the SWV record button, and then execute their code. After waiting the desired amount of time, pressing the debugger pause button will cause the IDE to review the profiling data and display it in the statistical profile tab, as in Figure 1. The developer can now analyze the code behaviour and determine if the code is behaving as expected or requires some additional tweaking.

The statistical profiler provides a powerful, yet simple, view into how the microcontroller is executing code. The easiest statistic to get out of the viewer is the processor load. As real-time

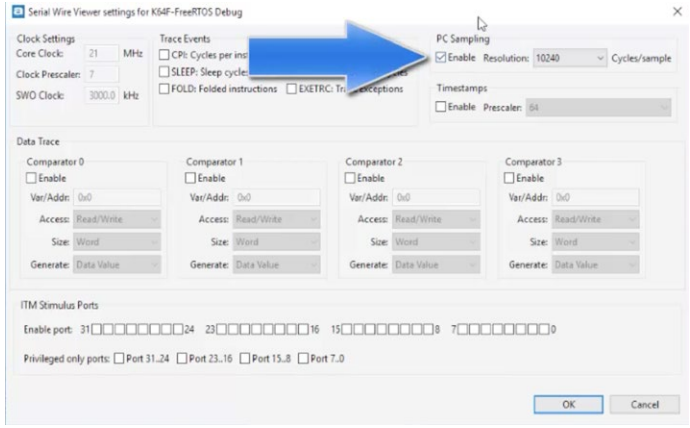


Figure 3. *Enabling PC sampling*

developers, we need to be very careful not to overload the processor much beyond 70%. With every additional 10% increase in load, the complexity and time required to add new features doubles.

Jacob Beningo is an embedded software consultant who currently works with clients in more than a dozen countries to transform their businesses by improving product quality, cost and time to market. He has published more than 200 articles on embedded software development techniques, is a speaker and technical trainer and holds three degrees which include a Masters of Engineering from the University of Michigan. Feel free to contact him at jacob@beningo.com, at his website www.beningo.com, and sign-up for his monthly Embedded Bytes Newsletter here.

HV BATTERY STACK MONITOR ENABLES ADVANCED AUTOMOTIVE DRIVES

By Greg Zimmer, Linear Technology

Large scale battery-powered energy systems are being deployed at an increasing rate, thanks to technology advances motivated by the demanding electric vehicles (EV) and hybrid/electric vehicles (HEV) market and further exploited by collateral markets, such as backup and carry-through energy storage. Tesla Motor's proposed Powerwall illustrates the very real potential for large-scale high power battery systems.

Innovation in batteries and battery chemistry have played an important role, however, and most advanced batteries require careful monitoring and control to maintain their capacity, life and safety. Furthermore, tens or hundreds of individual battery cells must be connected in series to support multi-kilowatt-sized systems. So while the system may see the battery stack as a single power source, each individual battery cell must be carefully managed. For this reason, large advanced battery packs have only been possible through sophisticated battery management electronics.

In the role of battery cell manager, battery management electronics have three important tasks.

- First, monitor the state-of-health (SOH) of each battery cell, which is usually determined by monitoring cell voltage, current, temperature and operational history.
- Second, control the state-of-charge (SOC) for each battery cell by controlling the charge, discharge and balancing of every cell in a system. Balancing involves adding charge to, or removing charge from, each cell in the pack, independently of the overall charge/discharge profile, to keep all cells withing a specified SoC range.
- Third, continuously confirm its own proper operation, as it would be unacceptable for the electronics to miss a potentially abnormal battery condition without informing the system. This last task is a critical element for functional safety.

Many years ago, Linear Technology recognized the difficult electronic challenges of battery management and developed a series of integrated circuits, known as multicell battery stack monitors. A battery stack monitor connects directly to a group of series connected battery cells; the primary function is to measure voltage on each cell, but it has evolved to include an ever increasing set of functions. Battery stack monitors are designed to be connected together such that they can monitor very long, high voltage battery strings.

The first such battery stack monitor was the LTC6802 which includes the ability to measure up to 12 Li-Ion cells with 0.25% maximum total measurement error, within 13msec. Many LTC6802 devices can be connected in series, to enable the simultaneous monitoring of every cell within very long, high voltage battery strings (Figure 1). Its designers have since followed the LTC6802 with the LTC6803, LTC6804 and now, the most advanced multicell battery monitor, the LTC6811.

This article continues by describing how the essential features of a battery-stack manager have evolved over time – click for pdf.

CFA AND VGA IMPLEMENT SIMPLE SIGNAL GENERATOR OUTPUT STAGE

BY DAVID HUNTER, ANALOG DEVICES

In the past, the most difficult part of signal generator design was the output stage. Now, a small, low-cost stage can be implemented by pairing a variable-gain amplifier (VGA) with a current-feedback amplifier (CFA). This design provides 20 MHz bandwidth, with 22.4-V (+39 dBm) amplitude into a 50-Ω load.

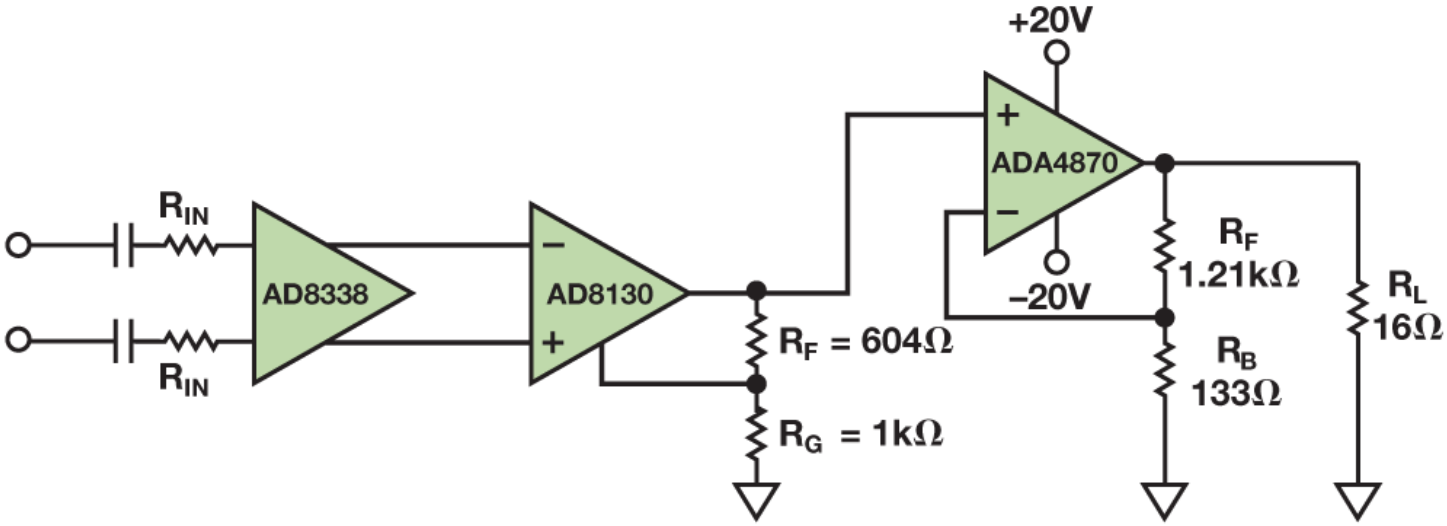


Figure 1. *Signal generator output stage*

The signal, which can come from a DAC for a complex waveform, or from a direct-digital synthesizer (DDS) for sine-wave generation, usually requires attenuation or gain. A typical signal generator offers an output amplitude range of 25 mV to 5V, a 46-dB adjustment range. The AD8338 low-power VGA provides an 80-dB programmable range. Under ideal conditions, the output amplitude of a classic signal generator could then range from 0.5 mV to 5V, without the use of relays or switched networks. The full range would be continuously adjustable, free of the discontinuities associated with switches and relays. In addition, eliminating the relays increases instrument lifetime and system reliability.

Many modern DACs and DDSs have differential outputs. With its fully differential interface, the AD8338 provides a natural fit. For a sine-wave application, the DAC would be replaced with a DDS. A major feature of the AD8338 is the flexible input stage, which manipulates the input currents using the "H-Amp" topology invented by ADI Fellow Barrie Gilbert. This design uses feedback to balance the input currents while maintaining the internal nodes at 1.5V. Under normal conditions, using the 500-Ω input resistors, the maximum 1.5-V input signal produces a 3-mA current. If the input amplitude were larger, say 15V, a larger resistor would be connected to the "direct" input pins. This resistor is sized such that the same 3-mA current is obtained.

The power of the input-VGA is that its total gain range can be located around different set points. Many commercial generators only provide a 250 mWrms (+24 dBm) maximum output power into a 50-Ω load (sine-wave). This is not enough to cover applications that need more output power, such as testing high-output HF amplifiers

or ultrasound pulse generation, for example.

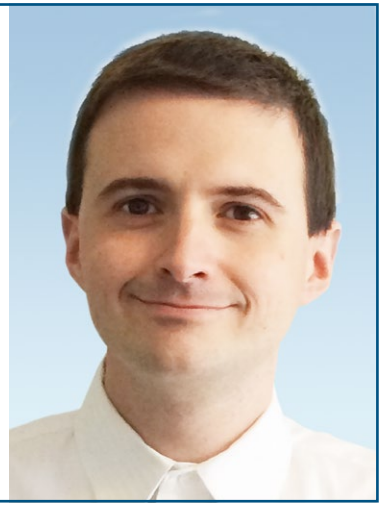
This no longer has to be a problem. The ADA4870 CFA can drive 1A at ±17V on ±20-V supplies. For sine-waves, it can produce a 23-MHz output at full load, making it an ideal front-end driver for the next generation of general-purpose arbitrary waveform/signal generators.

To optimize the output signal swing, the ADA4870 is configured for a gain of +10, so the required input amplitude is 1.6V. The ADA4870 has a single-ended input, and the AD8338 has a differential output, so an AD8130 differential receive amplifier, with its 270 MHz gain-bandwidth product and 1090-V/µsec slew rate, provides both the differential-to-single-ended conversion and the required gain. The AD8338's output is constrained to ±1.0V, so the AD8130 must provide an intermediate gain of 1.6 V/V. When combined, the three devices form a complete signal generator output stage.

Reference

Two new devices help reinvent the signal generator

David Hunter *[david.hunter@analog.com] is an applications engineers in the Linear Products Group at ADI's Wilmington campus. He joined ADI in 2006 as a field applications engineer working out of the Northwest Labs Design Center, serving the test and measurement field, as well as industrial customers. David graduated from Portland State University with a BSEE in 2007, specializing in RF Engineering. Prior to graduating, he published and co-authored papers on self-healing hardware systems and evolvable hardware. He is also an active amateur radio operator*



PARTIAL AND PRETENDED NETWORKING REDUCES CAN POWER CONSUMPTION

By Fritz Burkhardt and Giovanni Torrisi, STMicroelectronics

Minimizing energy consumption has become a major need for any new product design, including industrial and automotive systems that use the CAN bus. One way to reduce system energy consumption is to shut down elements not currently being used. To use this approach in CAN systems, however, requires re-imagining CAN controller architectures.

In recent years, significant efforts have been made within the industry towards reducing the energy footprints of many systems. For instance, in the automotive environment, efficient engine management and weight minimization of the vehicle bear the most significant potential for savings. But apart from factors including engine efficiency, vehicle weight, and aerodynamic drag, the power efficiency of the electronic control units has great potential as a field of activity for engineers designing to save energy. As a result, developers are also focusing on electronic functions in order to exploit every opportunity to reduce consumption.

The use of low-power electronic control units has in the past been particularly important for parked vehicles, in order to achieve maximum standby times with existing battery capacities. But current drain has now become important for driving vehicles, as well, because the electrical energy must be delivered by the combustion engine and thus has a direct influence on fuel consumption. And not only is the automotive industry facing the challenge of reducing its energy footprint: Global warming and the need of reducing emissions ask for better energy efficiency across many application domains.

Analyzing the electronics landscape in modern electronics quickly raises several questions. Are the functions offered by the different electronic control units (ECU) really required all the time and in every operating situation? Is the continuous current consumption of these modules really justified? Often, the answer is; no! Not, for instance, for convenience functions in the car such as seat electronics, trailer control units, or tailgate control units that are seldom operated or only required at specific times. Additional examples include door control units, auxiliary heating, sunroofs, and rear-view cameras.

On the other hand, it must be possible to activate these control units at any time in order to avoid any functional or convenience impairment. Networking, i.e. communication between different ECUs, can facilitate the job of selectively turning on only those modules needing to be activated at any given time. With networking to provide selective (partial) activation of the ECUs belonging to a complex system, there is considerable potential for energy savings.

Assume, for instance, that an automotive ECU has an average current drain of 100 – 200 mA and a car battery voltage of 14V. The potential savings amount to 1.4W to 2.8W for each idling control unit. Total energy savings for 10 nodes capable of partial networking therefore amount to an average of 15W without any negative impact on functions or convenience features. According to the established conversion formula, 40W of electrical power represent 1.0g of CO_2 emissions per kilometre. Thus, the introduction of partial networking leads to potential emission reductions of 0.375 grams of CO_2 per km.

But there are even more reasons why a partial network is an interesting approach. Consider, for instance, the charging of electric vehicles. Although charging requires a communication link to the supervising control unit,

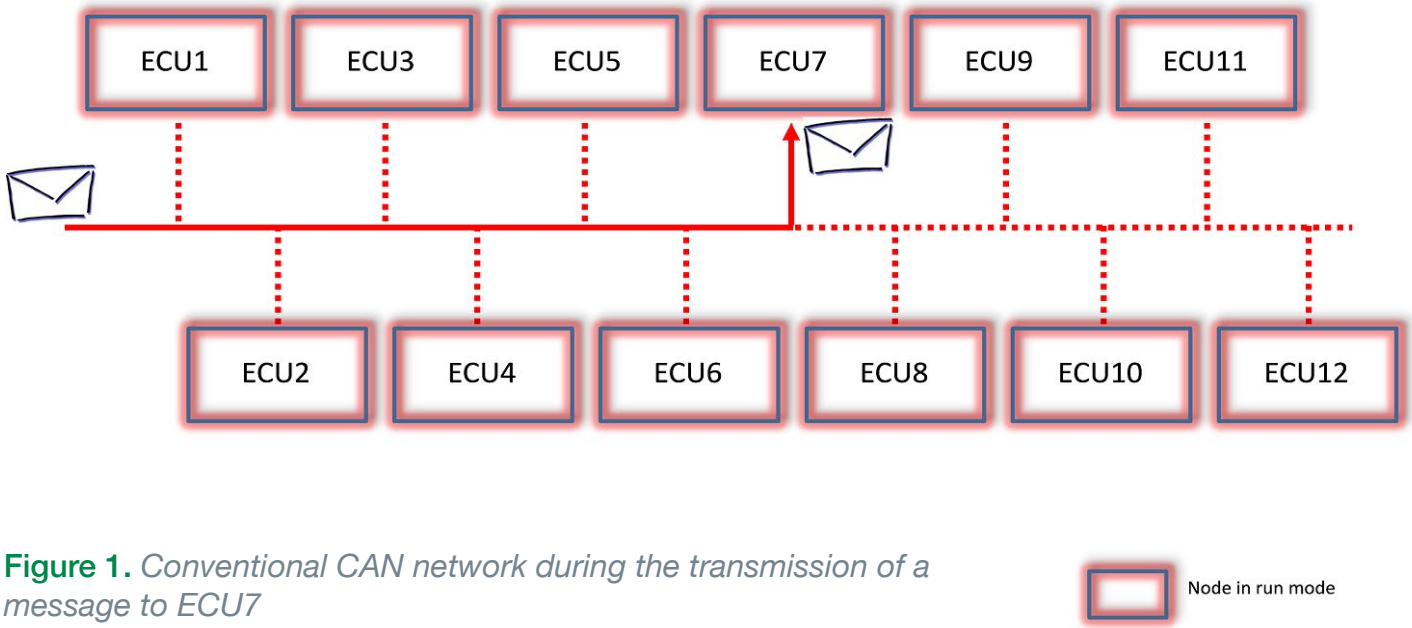


Figure 1. *Conventional CAN network during the transmission of a message to ECU7*

most of the control units connected to the bus are not required for this task and can thus be selectively powered down. The same is true for future application scenarios entailing data transmissions between a parked vehicle and mobile end devices.

These future use cases also result in increased requirements regarding the operating life of the components. This can be compensated to a certain extent by partial networking, resulting in reduced costs.

High speed CAN is the networking technology usually used in automotive and industrial applications where the bus runs from one end of an environment to another one. But there is a problem with selective activation when using the CAN bus. Although current CAN nodes already provide low-power modes (e. g. standby, sleep), they immediately wake up if any communication occurs on the bus. These low-power modes can thus only be used if all nodes connected to the bus are disabled simultaneously (so-called 'bus idle').

Simultaneous disabling of nodes is possible in the case for a parked vehicle (see Fig. 1). When a CAN message is transmitted on the bus, all connected controllers are awakened by the respective transceiver. But in the case of a moving vehicle these sleep modes are not helpful because at least some of the nodes on the bus must be continually active.

One possible approach for making use of CAN sleep modes in such situations is based on dividing the networks into sub-networks and disconnecting specific controllers from the supply voltage. Apart from the restrictions regarding the network layout, though, using multiple power supplies leads to additional overhead. Nonetheless, solutions of this kind are already in use today.

A more flexible approach is to have the ability to wake up specific controllers using dedicated, pre-defined wake-up messages. This ability allows partial networking, in which not all nodes need to be active at the same time... *The article continues by outlining the principles of partial networking and introducing the notion of pretended networking, to reduce power demand – click for pdf.*

MONOLITHIC JFETS ARE ALIVE AND WELL

BY STEVE TARANOVICH

High integration in today's analogue ICs is ever expanding, but there are time when a circuit designer needs to design a better differential stage to an amplifier, especially an audio amp or pre-amp, or a voltage controlled resistor, thermally stable follower, sample and hold or matched current sources or when the source is a very high impedance as in electrometer designs where super low bias current and low noise is critical.

Circuit design engineers need to look closely at the benefits of using discrete active devices like these. Jim Williams and Bob Pease were masters of using high-performance discrete active transistors to enhance their design performance when placed in critical areas of their system designs.

Linear Integrated Systems just introduced its LSJ689, a dual, P-channel JFET which is the complement to its LSK489, a dual, N-channel JFET. This new, dual, P-channel JFET has an excellent noise voltage spec at 1.8 nV/√Hz at 1 kHz with low input capacitance (8 pF typical). Plus there is near-zero popcorn noise in these devices. Although this type of noise has been virtually eliminated from ICs (note the term 'virtually'), there are occasions where any level of noise, no matter how infrequently it may occur, can interfere with sensitive circuit designs. The low offset voltage from very close matching of transistor characteristics is 20 mV maximum.

Circuit designers will find that tighter I_{DSS} (drain-source saturation current) matching to a 10% maximum as well as better thermal tracking (due to being on a monolithic die) can be obtained with these devices than by using individual JFETs.

Figure 1. *Linear Integrated Systems' LSJ689 dual, P-channel JFET has an excellent noise voltage spec at 1.8 nV/√Hz at 1 kHz with low input capacitance (8 pF typical).*

Applications

Bob Cordell wrote an excellent application note on High-Performance Complementary Input Stages. An example of one of his applications is a full complementary input stage fed into a push-pull second stage (Figure 2).

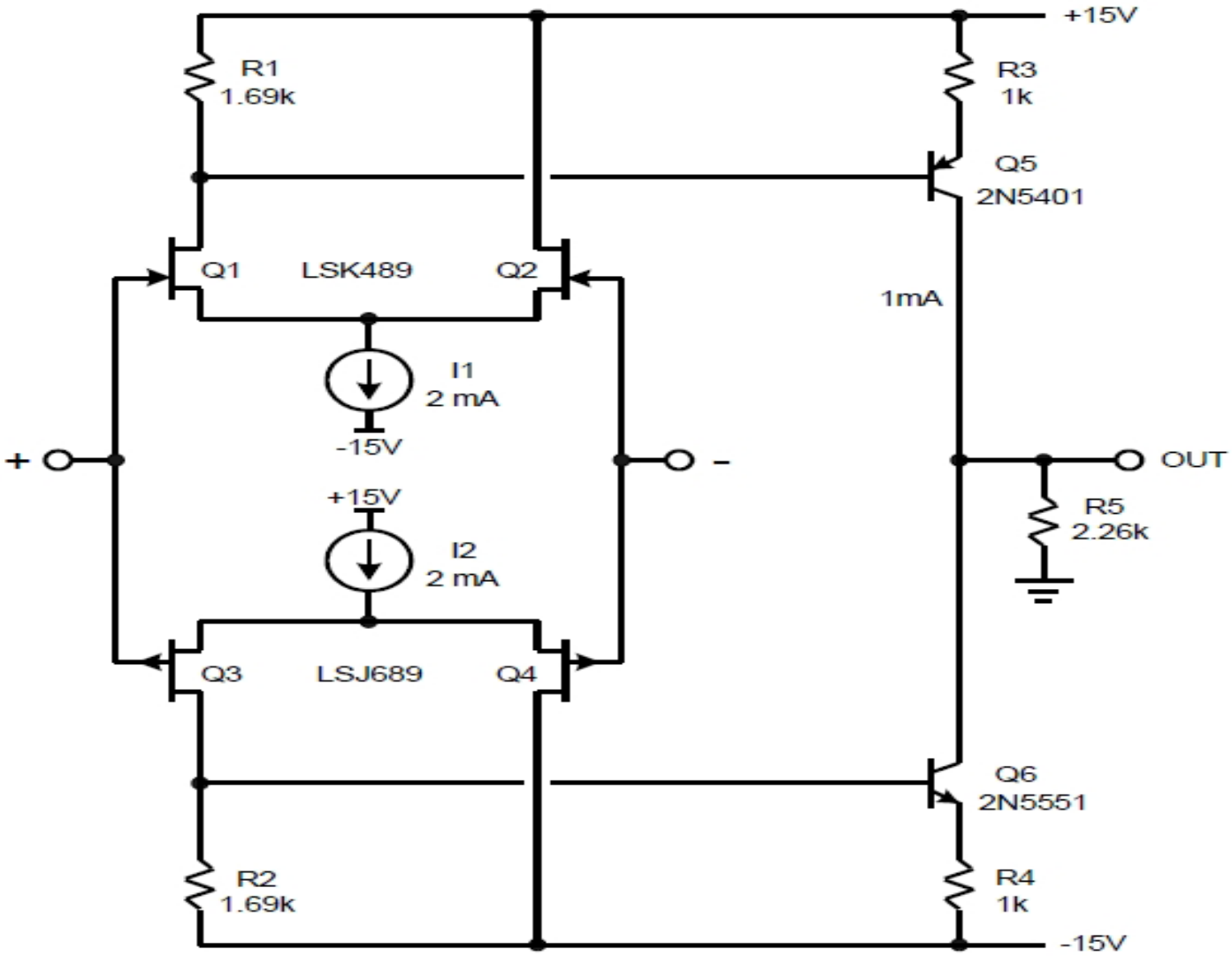


Figure 2. *This full complementary input stage feeds into a push-pull second stage (Q5, Q6) that will sum the outputs of the top (Q1, Q2) and bottom (Q3, Q4) input pairs.*

In Figure 2 and similar configurations, negative feedback is usually employed. Each long-tailed pair has a 2 mA current source (I1 and I2), connected to its associated power rail, powering it.

Packaging

The JFET pair is available in RoHS compliant SOT-23 6L, SOIC-A 8L and TO-71 6L package options. The LSJ689 SOT-23 6L and SOIC-A 8L packages are ideal for space-limited circuits in audio and instrumentation applications.

Linear Integrated Systems; http://linearsystems.com/

SEPARATION, SECURITY AND THE CONNECTED CAR

By Mark Pitchford, Lynx Software Technologies

No-one reading this article will need convincing of the seriousness of the security issues surrounding connected and potentially driverless vehicles. Evidence of the consequences of partial or incomplete security include Miller and Valasek's work, "Remote Exploitation of an Unaltered Passenger Vehicle" - the "Jeep Cherokee hack" (Reference 1).

Their example is not an isolated incidence. According to Senator Ed Markey (Re. 2), "Nearly 100% of cars on the market include wireless technologies that could pose vulnerabilities to hacking or privacy intrusions. A majority of automakers offer technologies that collect and wirelessly transmit driving history data to data centers, including third-party data centers, and most do not describe effective means to secure the data."

Most vehicles contain a variety of wireless technologies, including cellular, Wi-Fi, Bluetooth, Near Field Communication (NFC), and other RF communication. There is frequently a direct path from these wireless technologies to the central automotive bus of the vehicle, providing access not only to navigation, security, and other smart applications, but also to braking, steering, and cruise control systems.

Now that connection has become the norm, there is a significant learning curve for companies and individuals alike to understand the problems, and implement appropriate solutions.

The significance of attack surfaces and separation

The process standard ISO 26262 "provides an automotive-specific risk-based approach to determine integrity levels [Automotive Safety Integrity Levels (ASIL)]" (Ref. 3). The principle of the assignment of ASILs for various automotive systems implies an assumption of separation, so that the most critical systems on a vehicle cannot be compromised by less critical functionality elsewhere.

Traditionally, this was fine. ECUs were dedicated to their local function – engine control, ABS, or whatever – but an increasingly holistic approach to vehicle control meant increasing levels of interaction between each module.

A simple example of this interaction might be an automatic transmission, where the engine needs to tell the transmission what the engine speed is, and the transmission needs to tell other modules when a gear shift occurs. Traditionally such communications were handled by a traditional wiring loom, but as more and more similar interactions became necessary with the advent of features such as Cruise Control and Anti-lock Braking Systems, these dedicated looms because impossibly complex.

The answer to that conundrum lay in the development of vehicle networks, commonly in the format of a Controller Area Network (CAN). This network provides a medium for data exchange, allowing a uniform wiring architecture irrespective of the options specified on each individual car so that the appropriate modules can be simply "plugged in" to it.

While ever the vehicle remained isolated from the outside world, this connectivity between modules posed little threat to the security of the vehicle. Once the communications mechanisms on such a network were proven not to compromise the integrity of any systems using them, the various systems could be considered separated and so the principles of ISO 26262 remain upheld.

But the connected car changed all that. External access brings with it the potential for malicious outside influences to access any weak point, or "attack surface". Such an attack surface (Ref. 4) represents a significant risk even if it exists in a low or non-critical system, because the availability of the previously benign networks provides a portal to the highest ASIL systems. In stark terms, just because someone has attacked your car infotainment system doesn't mean they can't access the brakes.

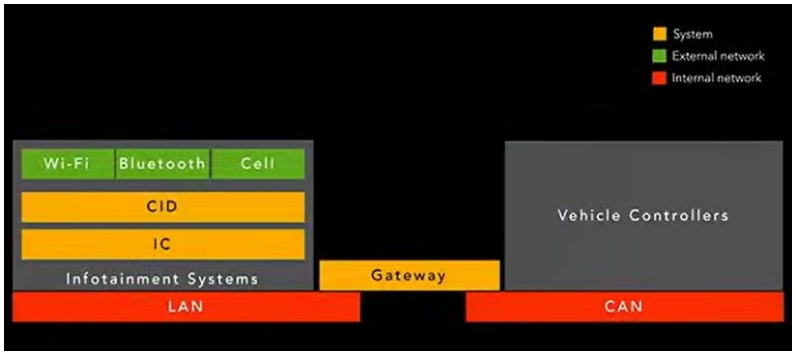


Figure 1. *Tesla's approach to separation is hardware based*

Clearly, then, a connected car will never offer the same level of security as an unconnected one. But for a connected vehicle to be considered safe and compliant with the principles of ISO 26262, it is imperative that attack surfaces are minimised, and that separation between systems is optimised.

Hardware based separation

The Tesla Model S uses a physical (LAN-CAN) gateway box to isolate the infotainment system from the safety-critical vehicle controller (Figure 1). The gateway box implements a structured API which supports a limited range of commands between the two networks, meaning that if the safety-critical vehicle controllers are to be accessed then a detailed knowledge of that API is required. It has not, however, proved to be entirely secure (Ref. 5) perhaps showing how difficult a challenge the connected car may be. Almost as importantly, it also introduces a considerable hardware cost overhead.

Software based separation

Although the Tesla system represents an effective approach to separation, if a similar or better solution can be found through software then it is likely to be more cost effective.

Search for the phrase "embedded hypervisor" on any popular automotive electronics site, and it would be easy to suppose that each of the many offerings is equivalent. To explore that notion a little further, consider a similar system to that of the Tesla, abstracted for this purpose and deploying a hypervisor instead of hardware separation (Figure 2).

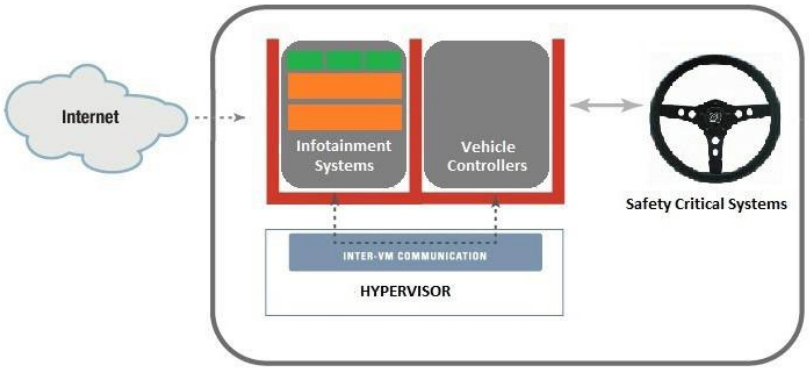


Figure 2. *An abstracted automotive system shows the importance of separation*

The hypervisor functionality is important, because it allows the system to mirror the Tesla in permitting restricted communication between two very different applications (Virtual Machines, or VMs) – one to handle the vehicle controllers, and the other the infotainment systems. A similarly obscure and structured API to that deployed in the Tesla would also make sense here.

But as far as the security is concerned, it is imperative that even if the outfacing infotainment VM is hacked and compromised, the vehicle controller VM is not vulnerable. If the VMs are to be truly separated rather than conjoined by the hypervisor, it is therefore vital that the attack surface is made as small as possible by minimizing the resources shared between them.

This article continues with a discussion of hypervisor and kernel structures, and how they may best be applied to maximize security. Click for pdf

ASN FILTER SCRIPT: A NEW PARADIGM IN BESPOKE FILTER DESIGN

By Sanjeev Sarpal, Advanced Solutions Nederland

The ASN Filter Script programming interface forms part of the ASN filter designer design tool, allowing designers a simple route to interactively designing bespoke filters, by entering their specifications as simple symbolic mathematical expressions.

Editor's note; Earlier in 2016 we carried an item on ASN's Filter Designer Tool, which attracted considerable attention from EDN Europe readers; that report noted; ...the package, for IIR and FIR filter design, offers and intuitive route to implementing digital filters that [ASN claims] represents the first significant advance in this class of tools for many years...a Windows-based package that assists with design of filters, primarily for implementation on processor targets, but also supporting floating point desktop algorithm development... structured to use an intuitive input approach that largely dispenses with entering parameters in text fields. Here, company director and algorithms and analytics specialist Sanjeev Sarpal describes an alternative method of executing filter design that also largely bypasses the high level of filter-specific expertise required by some conventional tools

The unique design experience offered by the tool enables users to create, analyse and verify their filter designs in a real-time interactive way, without the need of any complex mathematics. This new concept supersedes existing paradigms where design production was time consuming and restrictive.

Symbolic mathematics

ASN Filter Script allows designers to implement symbolic mathematical expressions directly. These may be definitions taken directly from textbooks, technical standards or even reference designs. As an example of simplicity and power of the language, consider the design of the following 2nd order IIR (infinite impulse response) notch filter, expressed as a conventional transfer function (above).

$$H(z) = \frac{1 - 2\cos w_c z^{-1} + z^{-2}}{1 - 2r\cos w_c z^{-1} + r^2 z^{-2}}$$

This transfer function may be simply mapped into the Filter Script code shown below.

Real-time interactivity

The scripting language offers designers the unique and powerful ability to modify parameters on-the-fly with the so-called interface variables, allowing for real-time updates of the resulting frequency response.

The complete code for the aforementioned transfer function is shown overleaf, where the

```
wc=Twopi*fc/fs;

Num = {1,-2*cos(wc),1};      // define numerator coefficients
Den = {1,-2*r*cos(wc),r^2}; // define denominator coefficients
Gain = sum(Den)/sum(Num);    // normalise gain at DC
```

```
ClearH1;  // clear primary filter from cascade
interface r = {0,1,0.1,0.5};  // radius range
interface fc = {0, fs/2,fs/100,fs/4}; // centre frequency range

Main()

wc=Twopi*fc/fs;

Num = {1,-2*cos(wc),1};      // define numerator coefficients
Den = {1,-2*r*cos(wc),r^2}; // define denominator coefficients
Gain = sum(Den)/sum(Num);    // normalise gain at DC
```

interface variable definition precedes the Main () section of the code.

The scripting language itself supports over 40 scientific commands and takes the best aspects of Scilab (the open-source software for numerical computing), R (the language structured for statistical computing and graphics), and ANSI C; and embodying approaches such as those seen in other commercial products such as Matlab – providing the designer with a familiar and powerful programming language, while at the same time allowing designers to implement complex symbolic mathematical expressions for their applications.

ASN Filter Script IDE

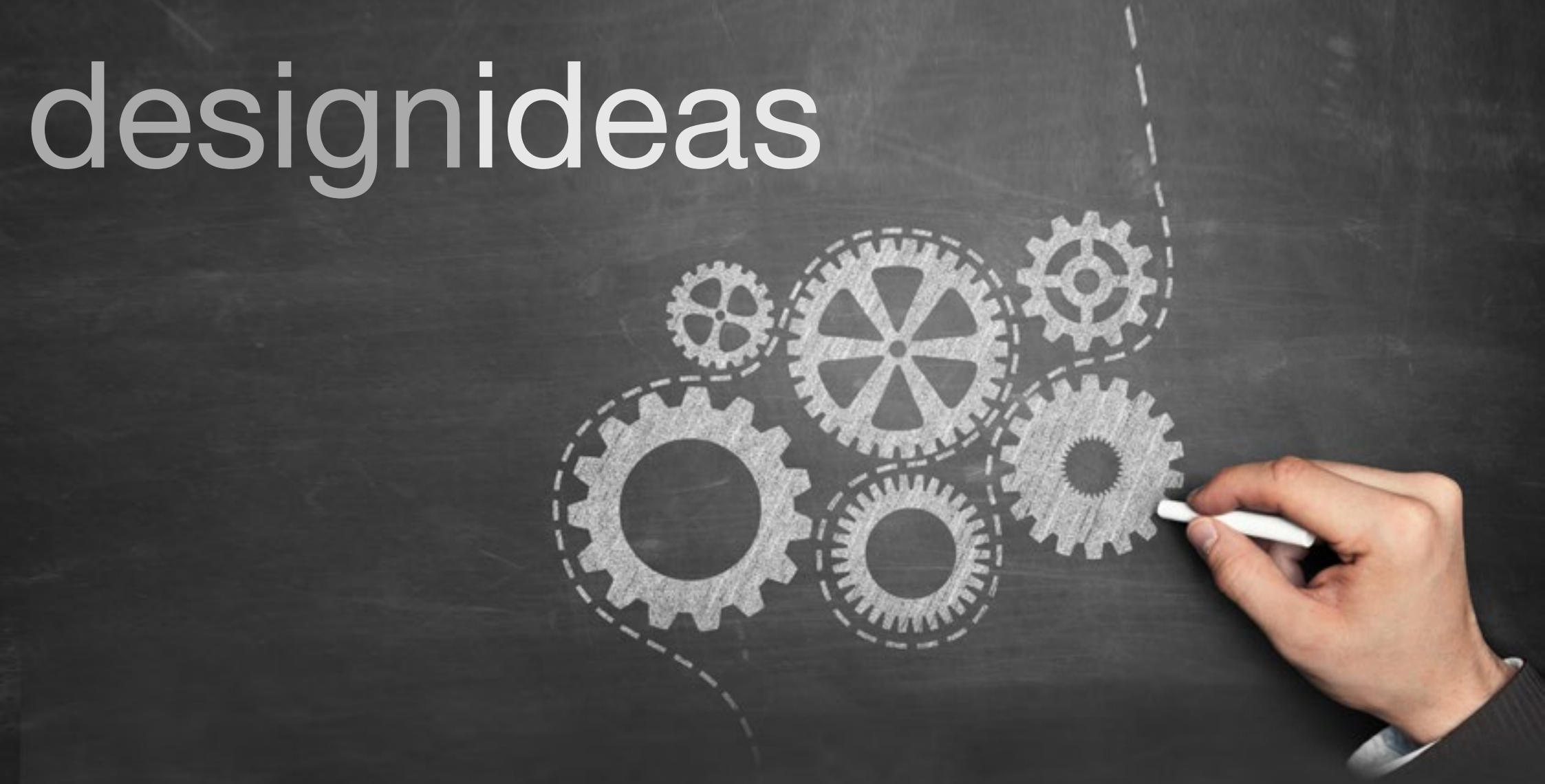
All developed code may be run within the tool's IDE (integrated development environment), providing designers with a user-friendly development environment with all of the necessary functionality needed to successfully optimise the transfer function for the application considered. The IDE is fully compatible with the ASN Filter designer's signal analyser, allowing designers to concoct a test signal and modify the design parameters on the fly - where, the effects on filtered output test signal can be seen in real-time.

Video clips on the tool are here and (in animated form) here.

Advanced solutions Nederland; www.adv-solned.com

Find Filter Design Tools on EETsearch

designideas



- Iterated-map circuit creates chaos
- Charge-pump topology doubles voltage, breaks DC path

Iterated-map circuit creates chaos

By Lars Keuninckx

The Design Idea circuit shown below is a simple implementation of an iterated unimodal map, reminiscent of the logistic or Verhulst map encountered in the study of nonlinear dynamics. It is useful to show chaotic discrete-time dynamics to students, or as a random number generator.

Specifically, the circuit implements:

$V_{k+1} = rF(V_k)$

where F is a nonlinear unimodal function (a “bump”), implemented by the circuit in the dashed box. The response of this circuit is shown in the Vout vs. Vin plot, Figure 1.

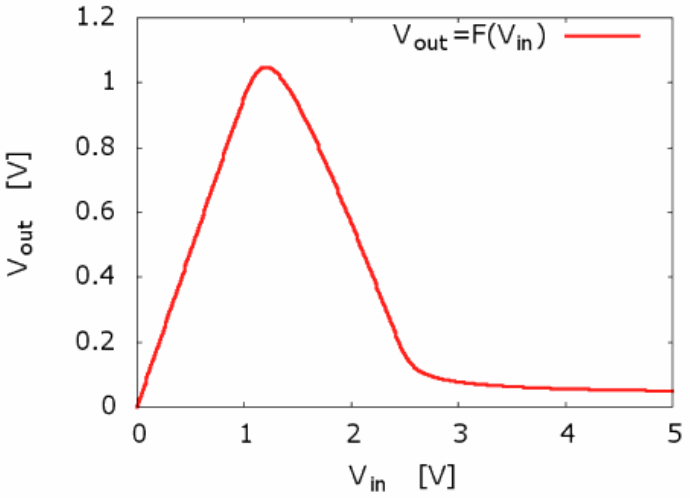


Figure 1. *Response of the Q1 unimodal function circuit*

r is a gain factor provided by U1b. U1a and U3a are simply buffers. During the low phase of the clock signal, the output voltage of the nonlinear function is stored on C1. When the clock switches to high, this voltage is transferred to C2, and then used as the next input to the unimodal function. The supply voltage is 12V. S3 (¼ 4066) is used as an inverter.

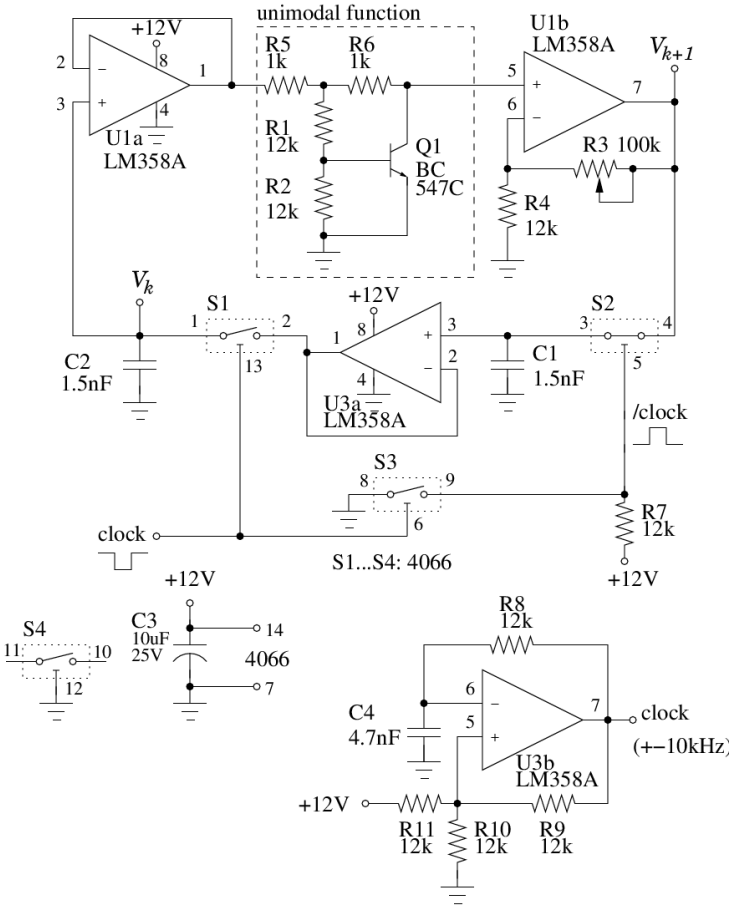


Figure 2. *Schematic*

For low gain settings (r), the iterates have the origin, zero volts, as stable equilibrium: V* = rF(V*). By increasing the gain, the circuit moves from a stable equilibrium to n-periodic oscillations. The iterates of an n-periodic oscillation can be seen as equilibria of the n-iterated map, e.g.,

$$V^* = rF(rF(rF(V^*)))$$

for 3-periodic oscillations. This is shown in the first oscilloscope screenshot, Figure 3, for r=4.7.

Figure 3. *Behaviour for r=4.7 (red trace: Vk, blue trace: clock).*

Further increasing the gain leads to chaos. Each initial condition or starting voltage in theory leads to a never repeating sequence of iterates. The logistic map

$$x_{n+1} = rx_n(1-x_n)$$

is the best known model for such an iterated chaotic system, and uses a parabolic function. However, it turns out that any unimodal map, including discontinuous maps such as the mod-map, or non-smooth maps such as the tent map, also lead to chaos, hence the use of the simple circuit around transistor Q1.

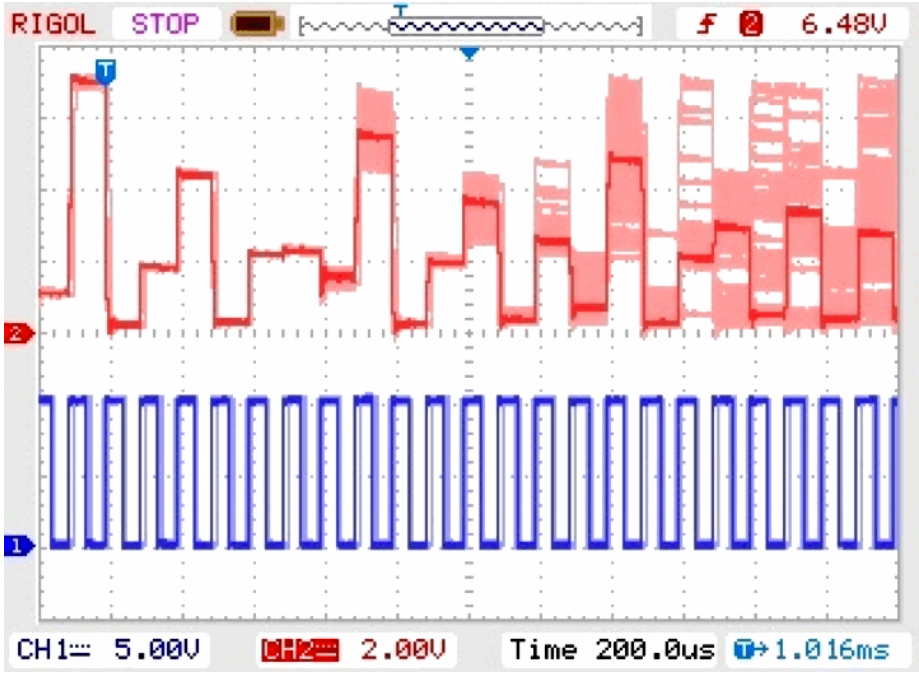
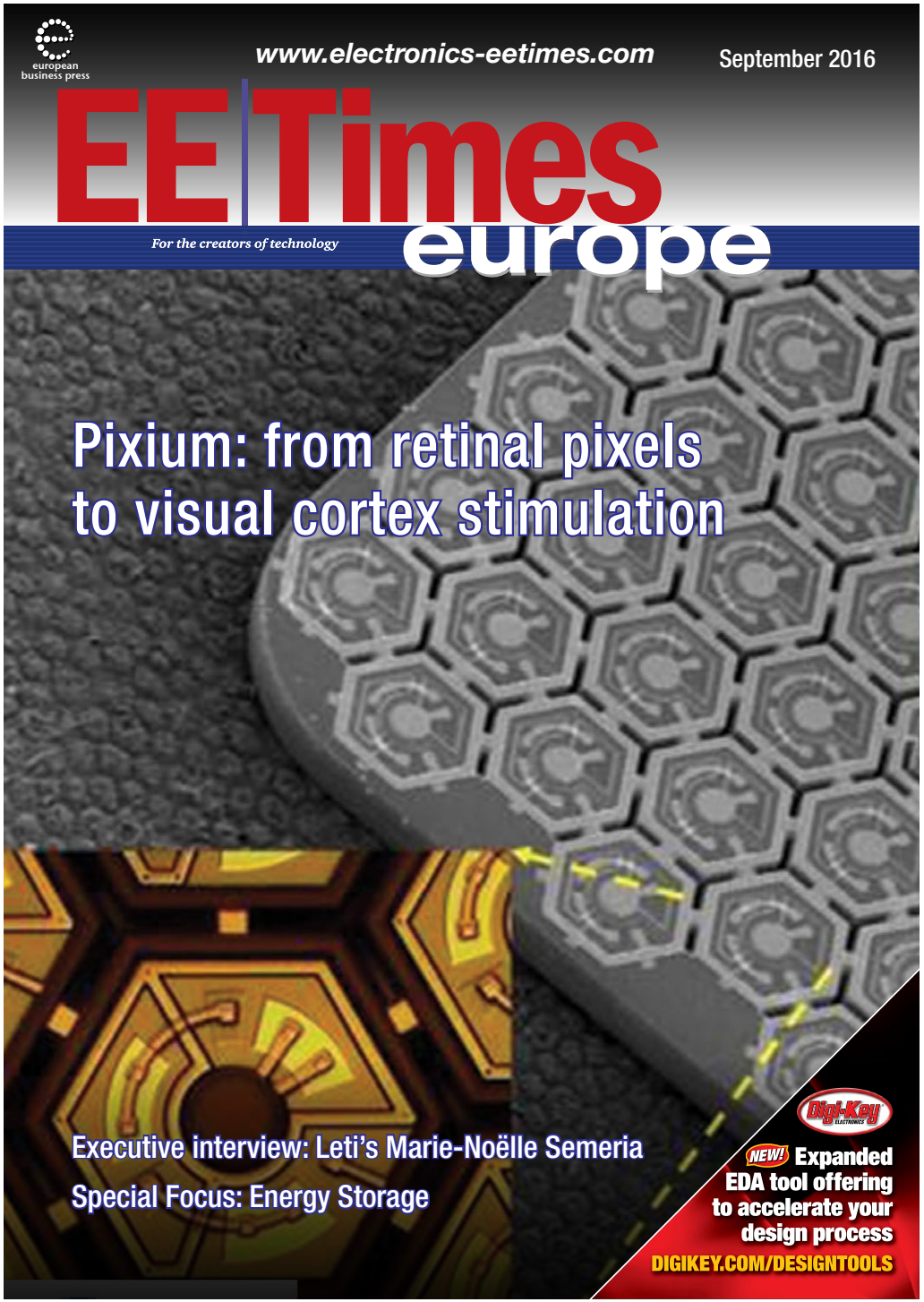


Figure 4. *Behaviour for r=6.7, made by setting the scope persistence to infinity and triggering as close as possible to the top of the voltages obtained.*

Figure 4 shows the circuit's behaviour for r=6.7, made by setting the scope persistence to infinity and triggering as close as possible to the top of the voltages obtained.

Figure 4 shows a key property of deterministic chaos: sensitive dependence on initial conditions. Nearby (but slightly unequal) initial conditions (trigger voltages) lead to diverging iterate series after a just a few updates. Loosely speaking, there is a kind of “event horizon”. It is easy to predict the next iterate, but impossible to predict, say, the twentieth, from the current state, because we then have to know the initial condition with very high precision. It is important to note that even if this system could be made noiseless (as for the theoretical logistic map), it would output a chaotic sequence.
As for applications, the circuit can be used as a random number generator, real-life demonstrator of chaos, or just to flabbergast the local lab smartie who claims they’ve seen every circuit in the book.

Lars Keuninckx *spent over ten years in industry, designing automotive, industrial, and medical electronics, before returning to college to work on a physics degree. His interests include applications of nonlinear dynamics in electronic circuits, chaos, and neural networks. He recently obtained a PhD in engineering at the Applied Physics Research Group (APHY) of the Vrije Universiteit Brussel on the applications of delay systems and reservoir computing.*



Charge-pump topology doubles voltage, breaks DC path

By Michael Dunn, EDN

I once needed a voltage doubler circuit with no DC leakage path between input and output, and ended up devising this unusual 556- (dual 555 timer) based circuit with a "floating" voltage output.

Despite some shortcomings, the 555/6 are remarkably versatile chips. Here, I take advantage of the high-current output drivers (>200 mA) in what could be called a push-pull configuration.

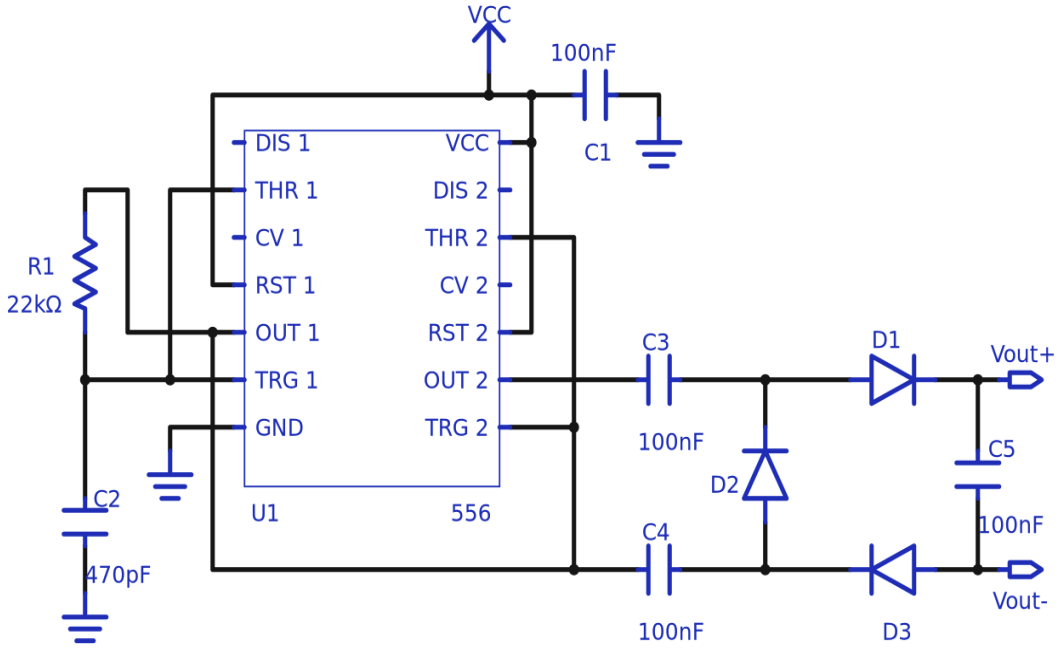


Figure 1. *The pseudo-floating charge-pump voltage doubler,*

The left half of U1 is connected so as to generate a 50% duty-cycle output. OUT1 drives one leg of the charge-pump, but also feeds the right half of U1, which is connected to simply invert its input. OUT2 drives the other leg of the charge-pump, 180° out of phase from OUT1.

The resulting square wave across D2 has an amplitude of 2·VCC, which D1, D3, and C5 convert to a DC output.

The output isn't truly floating, in that AC current could flow from input to output if they are at related potentials. However, there is no DC path from input to output, something I absolutely needed in the overall design, a DC solid-state relay.

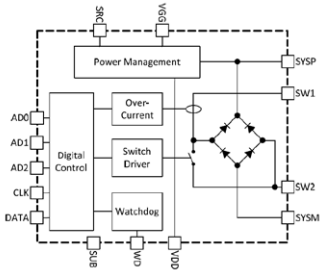
Component values will depend on the required output current and the switching frequency. To minimize losses, diodes could be Schottky.

productroundup

productroundup

Solid state relays for self-powered control systems

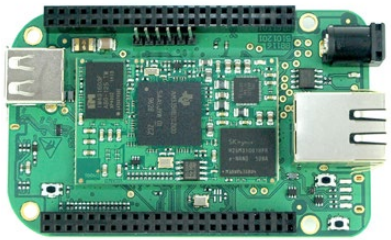
Semtech's TS13102 and TS13103 solid state relays in the Neo-Iso product range have added features to aid design of energy-harvesting and self-powered control systems in Internet of Things (IoT) applications, such as smart thermostats, alarm panels, factory automation systems, and smart controls. The TS13102 solid state relay can autonomously harvest energy even when its switch is closed and without the assistance of a microcontroller. The harvested energy is stored in a system capacitor (Csys) and can be shared across multiple channels in the system driving several loads.



Complete article, here

BeagleCore: an embedded industrial/IoT computing module, in distribution

Distributor Conrad Business Services has added an open-source module and starter kit based on the BeagleBone Black, as a rapid development tool. The BCM1 embedded computing module and BCS1 starter-kit will be exclusively available to Conrad's customers world-wide. Heavily based on the BeagleBone development board, these devices provide small, simple and powerful building blocks for creating and testing new technologies for industrial and Internet of Things (IoT) applications. Conrad offers them as suited for professional and industrial embedded solutions.



Complete article, here

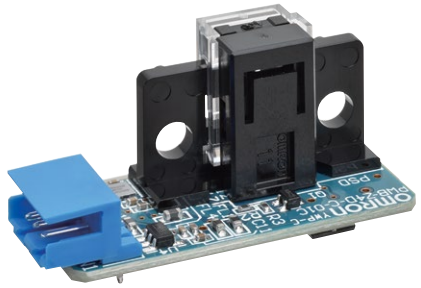
BBC micro:bit gets Segger's J-Link debug firmware support

Segger (Hilden, Germany) has introduced J-Link support for the BBC micro:bit providing students a path to using a production grade IDE for their next micro:bit project. Segger offers the capability to upgrade the firmware on the BBC micro:bit DAPLink to a J-Link OB (On Board). This firmware makes the on-board debug solution on the BBC micro:bit compatible to J-Link, allowing users to take advantage of all J-Link features such as ultra fast flash download and debugging speeds and the free-to-use GDBServer as well as application development using an IDE.

Complete article, here

Micro-displacement sensor resolves 10 microns

An optical micro-displacement sensor from Omron Electronic Components Europe is capable of resolving 10 microns – one tenth the diameter of a human hair or the thickness of a coat of paint. The high resolution of the Z4D sensor suits it for paper thickness and multi-feed detection office equipment and ATMs, as well as travel detection in industrial automation systems, consumer electronics and other applications. The Z4D-C01 locates target objects optically without the need for contact, up to 6.5mm away from the sensor.



Complete article, here

productroundup

ADI uprates 6GHz DAC with on-chip synthesiser

Analog Devices' AD9164 is a digital to analogue converter that spans audio to 6 GHz frequencies; it has the same conversion specification as the recently-announced AD9162, and also includes an on-chip direct digital synthesizer; it offers more accuracy in a smaller footprint for diverse applications ranging from radar to smartphone testing. The AD9164 D/A converter supports high resolution radar images for designers of military and commercial radar while reducing solution component count. For designers of precision instrumentation it device ensures improved accuracy as well as speed of test.

Complete article, here

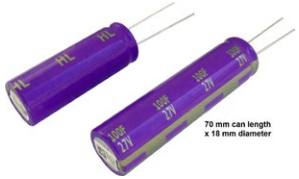
Thermal-imaging DMM, in distribution

Distributor Conrad Business Supplies has the thermal multimeter 279 FC from Fluke, that combines a thermal imager with a fully-featured true RMS digital multimeter to enable faster and more thorough troubleshooting with a single tool. The 279 FC's thermal multimeter measures AC/DC voltage, resistance, continuity, capacitance, diode test, min/max, and can carry out frequency tests. At the same time, the integrated thermal imager allows the 279 FC to quickly and safely check for hot spots in fuses, wires, insulators, connectors, splices, and switches.

Complete article, here

50 & 100F electric double layer caps offer 100k cycles

Panasonic's "Gold Capacitors" offer long life and superior performance over secondary batteries for auxiliary power applications; they have low resistance, ultra-fast charge and discharge cycling that suits backup power supplies for servers and solar applications. HL Series Electric Double Layer Capacitors (ELDCs) offer low resistance combined with guaranteed long life over a wide temperature range, down to -40C and extending to +65C. They are wound radial lead type devices, which achieve far better capacitance compared to aluminium electrolytic capacitors (up to 1,000 times greater) and superior charge and discharge performance compared to secondary batteries.



Complete article, here

GPS-free, LoRa-based positioning for IoT

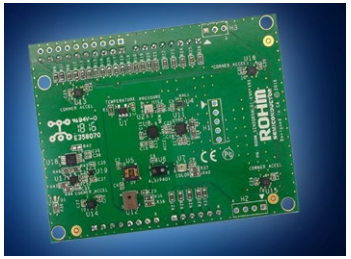
CSEM (Neuchâtel, Switzerland) has proposed the first commercial solution based on Semtech's LoRa technology for GPS-free geolocation of connected devices. This allows the geographical tracking of LoRaWAN end-nodes without any material impact on bill of materials or battery life. Semtech, developer of LoRa, recently announced the addition of geolocation functionality, which is compatible with all LoRaWAN end-nodes and second generation gateways. CSEM applied a statistical algorithm to Semtech's time-difference-of-arrival (TDOA) approach to calculate the position of LoRaWAN nodes. The pilot deployment used for development and testing of the solver was composed of 10 gateways located in and around the city of Neuchâtel. As a result, CSEM today has announced its own LoRa-based solver allowing tracking of any LoRaWAN node using existing second generation hardware.

Complete article, here

productroundup

Sensor shield evaluation kit, by Rohm, in distribution

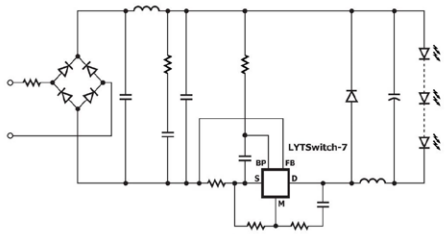
Distributor Mouser has Rohm Semiconductor's SENSORSHLD1-EVK-101 Sensor Shield evaluation kit, integrating 10 onboard sensors into a board with an Arduino Uno R3-compatible layout for prototyping and initial set development for IoT and machine-to-machine (M2M) applications, the Sensor Shield includes: BDE0600G analogue temperature sensor; BU52014HFV omnipolar hall switch sensor; KX122 digital accelerometer; KXG03 digital gyroscope and accelerometer; ML8511A analogue ultraviolet (UV) light sensor; RPR-0521 digital ambient light sensor and proximity sensor; BH1745 digital colour sensor.



Complete article, here

PI tunes dimmable LED drivers for cost & widest market appeal

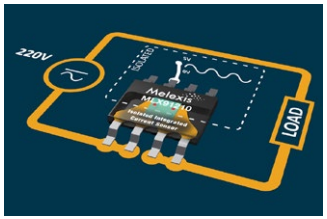
The latest generation of Power Integrations' non-isolated driver ICs for LED light bulbs, LYTSwitch-7, is a single-stage, non-isolated, TRIAC-dimmable, buck topology LED driver IC family. Capable of delivering up to 22W without a heatsink from an SO-8 footprint, these high-efficiency devices are suitable for bulbs, tubes and fixtures. LYTSwitch-7 designs do not require bleeders; employing simple, passive damping for TRIAC management and an off-the-shelf, single-winding inductor, reducing component count to 20, vs. 35 parts for typical dimmable LED driver boards.



Complete article, here

Hall-effect current sensing replaces shunts

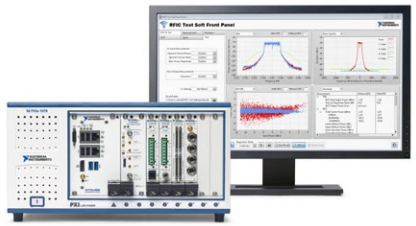
These high speed isolated calibrated current sensors are presented as an effective alternative to conventional shunt based solutions; standard-footprint packaged ICs simultaneously offer 100 kHz bandwidth, high accuracy and crosstalk resilience. Melexis' MLX91210 family of integrated sensors, operating from a 5V supply, have current sensitivity levels down to 26.7 mV/A and support linear current measurement ranges that span as far as ±75A corresponding to 30 ARMS current. The integrated Hall-effect current sensors have extremely low resistive current-path losses (0.8 mΩ for the SO8 and 0.7 mΩ for the SO16) and provide high voltage isolation.



Complete article, here

NI updates its Vector Signal Transceiver to 2nd-gen, 1-GHz b/w

The NI PXIe-5840 module is presented as the first 1 GHz bandwidth VST: software-designed instrumentation to stay ahead of complex and rapidly changing wireless technologies and requirements. The NI PXIe-5840 combines a 6.5 GHz RF vector signal generator, 6.5 GHz vector signal analyser, high-performance user-programmable FPGA and high-speed serial and parallel digital interfaces into a single 2-slot PXI Express module. With 1 GHz of bandwidth, the latest VST is suited for test of 802.11ac/ax devices, mobile/IoT devices, 5G design and test, RFICs, and radar prototyping.



Complete article, here

productroundup

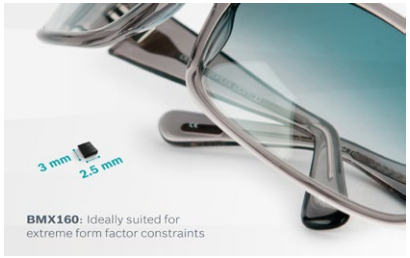
USB oscilloscopes add waveform generators

USB and bench oscilloscopes may include an AWG (arbitrary waveform generator). TiePie Engineering 's latest model, HS5-540, uses what the company calls CDS (Constant Data Size) architecture. It's closer to a traditional sampling AWG than to a DDS architecture. But, it differs in that its clock can change frequency to change sampling rate up to 240 Msamples/sec with stable signals: jitter is specified as less than 50 psec rms. AWG basic specs for the HS5-540 include; total harmonic distortion - 0.04 %; Jitter - 20 psec; signal frequency range - 40 MHz; memory size - 64 Mbytes; rise time - 8 nsec.

Complete article, here

Smallest 9-axis motion sensor

Bosch Sensortec claims to have the smallest 9-axis motion sensor, a low power design for smartphones, smart watches and other wearables: ultra-low power consumption helps extend usage intervals of battery driven devices, with uses including smart watch gestures, step counting, magnetic heading and device orientation. Pin- and register-compatible with the prior BMI160 for design flexibility, the BMX160 is a power-efficient 9-axis sensor in a 2.5 x 3.0 x 0.95 mm package, combining Bosch Sensortec's advanced accelerometer, gyroscope and geomagnetic sensor technologies.



Complete article, here

Single-chip Bluetooth Low Energy SoC from ST

STMicroelectronics' first Bluetooth Low Energy wireless System-on-Chip (SoC), BlueNRG-1 has been configured for high-volume applications in the Bluetooth Low Energy market through the combination of energy efficiency and strong radio performance. The BlueNRG-1 single-core SoC hosts a 32 MHz ARM Cortex-M0 core with 160 kByte of on-chip Flash memory for application-code and data storage besides the possibility to upgrade the ST Bluetooth Low Energy firmware stack. ST has employed ultra-low-power design with support for fast wake-up and sleep transitions, and sub-1µA standby current.

Complete article, here

Self-refresh DRAM on 'HyperBus' interface

Cypress Semiconductor is sampling a high-speed, self-refresh Dynamic RAM (DRAM) based on its low-pin-count (12-pin) HyperBus interface. The 64Mb HyperRAM serves as an expanded scratchpad memory for rendering of high-resolution graphics or calculations of data-intensive firmware algorithms in automotive, industrial and consumer applications. The devices operate with a read/write bandwidth of up to 333 MBps and are available in 3V and 1.8V supply voltage ranges. When paired with a Cypress HyperFlash NOR Flash memory, HyperRAM enables a simple and cost-effective solution for embedded systems where both the flash and RAM reside on the same 12-pin HyperBus. Traditional systems with an SDRAM and Dual-Quad SPI solution require upwards of 41 pins on two buses for data transactions. The HyperRAM and HyperFlash solution reduces pin count by at least 28 pins, decreasing design complexity and lowering PCB cost.

Complete article, here

HAPTICS DEVELOPERS BRING SURFACES AND FREE SPACE TO LIFE

BY GRAHAM PROPHET

This short article outlines recent demonstrations I have been given of two – quite dissimilar – technologies in the "haptic feedback" arena. You should not think of this as a review: to amount to a review, I would need a longer period of using and getting to know each technology. One of them, at least, does require a certain amount of – if not skill – acquaintance or adaptation on the part of the user. If not a review, then, I might term it an impression: but in any event, both of these HMI (human/machine interface) technologies involve an experience unlike any other in the sector, and if you think either might be appropriate for your design, then hands-on experience is essential.

The first technology is that of Redux, based near Cambridge, UK. The company's tag line is that it "brings surfaces to life" - its specialism is in exciting bending waves in planar structures. For the purposes of the demonstration I witnessed, this is the surface glass of an LCD (or OLED) display panel – although, other surfaces are also feasible. Redux attaches transducers, typically magnetic or piezoelectric devices, to a panel and excites it to obtain interfering patterns of wavefronts on the surface of the panel, with two main objectives.

The first effect is to produce a region on the (typically) glass surface that, as a result of interfering wavefronts, is deflected at audio frequencies. Modulation of the waveforms driving the glass directly yields a loudspeaker. Generating audio from a planar surface is far from new (think of the classic Quad electrostatic loudspeakers, as just one example) but the technique employed by Redux is capable of simultaneously generating separate, independent, sound sources on a single panel – yielding stereo from an LCD screen, or the screen of a laptop.

(As an aside, an antecedent company to Redux, NXT, experimented some years ago with a loudspeaker technology that, in common with the diaphragm of an electrostatic speaker, used all-but-massless transducers – an array of 'piston' transducers were to be fed, in pulse mode, with digital waveforms and D/A conversion was to take place 'in the air'. This demonstrably worked but was never commercialised.)

To return to the screen of the phone, laptop, or full-size LCD – the technology scales across a wide range – the second effect is to produce localised haptic effects on the surface. Today's tablets typically include a simple haptic feedback effect; when a touch is detected a transducer generates a click which is felt over the whole device. Redux' technology can localise that effect, generating a sensation that is only perceived in a particular location; further, it can create the perception of outlines, edges and surface textures, selectively in areas of the surface. In the demonstration Redux presented, letters displayed on the LCD have perceptible (to touch) "edges": the user can detect them, and drag and drop them around the screen.

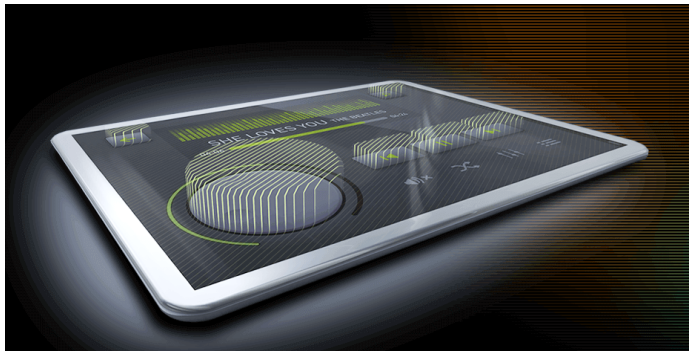


Figure 1. *Redux' technology gives feel and presence to 'soft' controls*

Further, in a recent extension of the technology, this effect can be made multi-touch. You can "find" a virtual button with one finger, tap it (this part is done with co-ordinated conventional capacitive touch sensing) to open ("popup")

a second region which, with another finger, you might use to adjust a variable value. The technology can impart different sensations to each of the zones.

Redux reports interest from a range of sectors including automotive – where positive, safe, reliable activation of functions, preferably without having to look, is desirable; mobile devices – where better sound can be produced from a small screen; and from industrial design where, with capacitive touch already in use, the haptics can provide added assurance of accessing and activating the correct function. Controls on a screen can be freed from fixed layouts; with an approximate landing of finger on screen, the control can be brought to the touch point and the localised feedback can give confidence that the intended action has been performed.

The actuators that have to be added to a panel range from moving-coil electromagnetic – you might use four for a laptop-size panel, or two for a smartphone – to piezo-electric patch-drivers for a very thin layout. The computational resources needed to calculate the waveforms to drive the actuators, and to interact with detected touches, is said to be modest; dual-touch operation can be handled by, the company says, an ARM Cortex-M4-class core.

Subjective bit

In the demonstration I saw, each of the usage examples described above was convincing, and easy to use. Virtual objects on screen – buttons, sliders or in the demo, letters of the Redux company logo, did have distinct edges and textures. The effect is surprisingly hard to describe; the "virtual edge" does not feel knife-edge sharp but is nevertheless unmistakable. The various use cases proposed seem attractive, for example operating controls on an automotive screen, on in medical or industrial scenarios where the distraction of looking at a screen is undesirable. Even without that requirement, the assertion that a touch screen can be more responsive and interactive seems borne out. Also, the audio generated from a flat panel seems of good quality – although, with the size and performance of the speaker elements provided in many portable, especially small, products, that should be an easy battle to win.

Touching the virtual in free space

My second haptic experience was provided by Ultrahaptics (Bristol, UK), which has pioneered the use of ultrasound to create "virtual" objects in open air.

Ultrahaptics' technology employs ultrasonic transducers in a phased array. The transducers are simple devices, similar to those used in automotive reversing-sensor applications. They radiate at 40 kHz, and the intended effect/information is imposed as a modulation on the 40 kHz waveform. Phasing the feeds to sensor in a rectilinear array generates interference and "beam-steering" effects that can be detected by the sense of touch.

Ultrahaptics alludes, at this point, to the extraordinary sensitivity of the human sense of touch; a fingertip swept across an extremely smooth surface can detect irregularities of molecular – almost atomic – dimensions. The 3D ultrasound field produces real and measurable – albeit very small – forces, and it is these that the hand can detect.

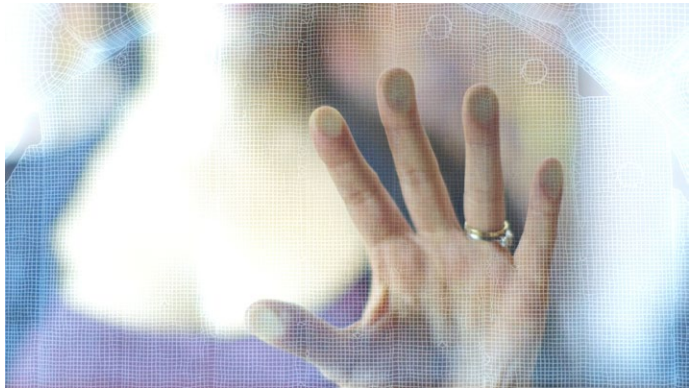


Figure 2. *Ultrahaptics' manipulation of ultrasound generates small but distinctive forces and contact sensations in mid-air.*

When considering use cases, Ultrahaptics notes the move to gesture-based control operation, and comments that there is an absence of feedback to that modality, other than some system-generated visual confirmation that an action has been initiated. Its technology, the company says, "makes virtual reality complete". In a typical application, you might place a hand into the (ultra)sound field. The system you seek to interact with would then detect its (the hand's) presence and confirm detection by setting up a sensation at the point of detection. You, the user, would then feel that you had "captured" the control field. A range of gestures is then available to command control actions; for example, Ultrahaptics shows "pressing" a virtual button by making a "patting" action – you can get a haptic "click" back on your palm as acknowledgement. Or, a circling motion with open palm "rotates" a volume control, for example.

Some of the company's proposed applications exploit the absence of touch. For example, in a medical instrument or control panel, hygiene might be aided by completely contact-free operation. The automotive industry, once again, is reported to have shown an early interest in the technology, to provide distraction-free operation of controls from the driving seat. You do not have to look for the location of a control; when it is the next expected action, place your hand in the approximate location and the control will come to you.

Further possible use cases come from the kitchen. The cook might operate controls on a hob or oven, with hands coated with ingredients. A related function is to provide a warning or virtual barrier: ceramic hobs remain hot for some time after use, with no indication of their temperature except a warning pilot light. Ultrahaptics suggests that its system could detect the approach of a hand, and set up a warning sensation to alert the user. The effect cannot set up a physical barrier, but it can operate as a "tripwire". The same principle could be applied to industrial or medical designs.

Subjective bit

Once again, there is a problem of describing a sensation that does not entirely relate to any other in normal experience. It is like a very light touch or pressure on the skin – but although very light, is unmissable. (The sensation can be varied by modulation, pulsing, and so on.) The capture/acknowledge process is positive, and a small amount of practice familiarises spinning or sliding controls. Ultrahaptics calls its "tripwire" scenario a "force field". While literally true – there is a force, in a field – you should not expect Star Trek-style traction or exclusion barriers: but as a reminder or alert, the proposition seems very credible. Likewise, the technology is not at a stage where you (or, at least I) can "feel" the shape of a complex virtual object in mid-air – although Ultrahaptics says it is working on this aspect. Edges and simple shapes can be discerned, though.

As a personal comment, I am slightly less convinced by some of the possible use cases. You might control a top-end audio system by gesture, for example. However, there is some satisfaction to be had from operating a solid physical switch or control designed with with good ergonomics; in the past, some brand values of end-equipment have rested on such factors. More specifically, the argument of not requiring to look away from the driving task to find, for example, a volume control on the automotive fascia seems to me a little overstated. We quickly learn where frequently-used controls are located and our hand reaches to them without looking. I may well be wrong on that and we may soon be gesturing freely at our dashboards: even if not, the basic premise of completing a feedback loop in virtual reality should offer ample options for new HMI experiences.

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